OpenRex

Variant: [No Variations]

27. 11. 2015
V1I1

CHECKED

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

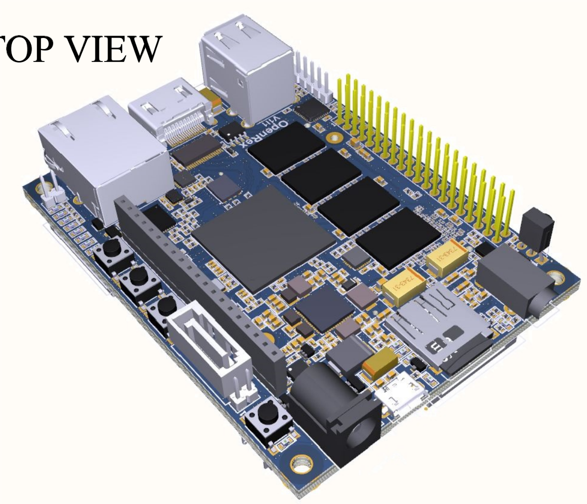
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

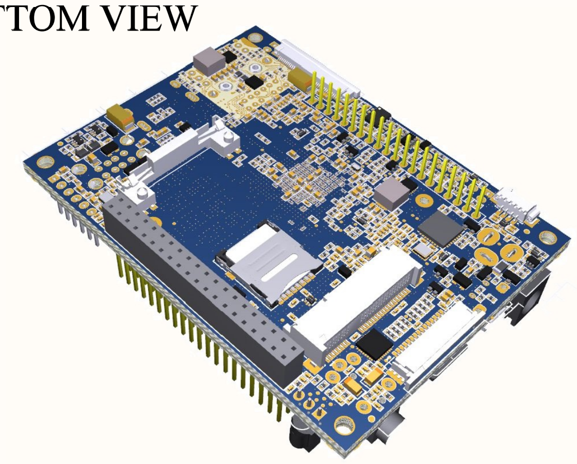
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW

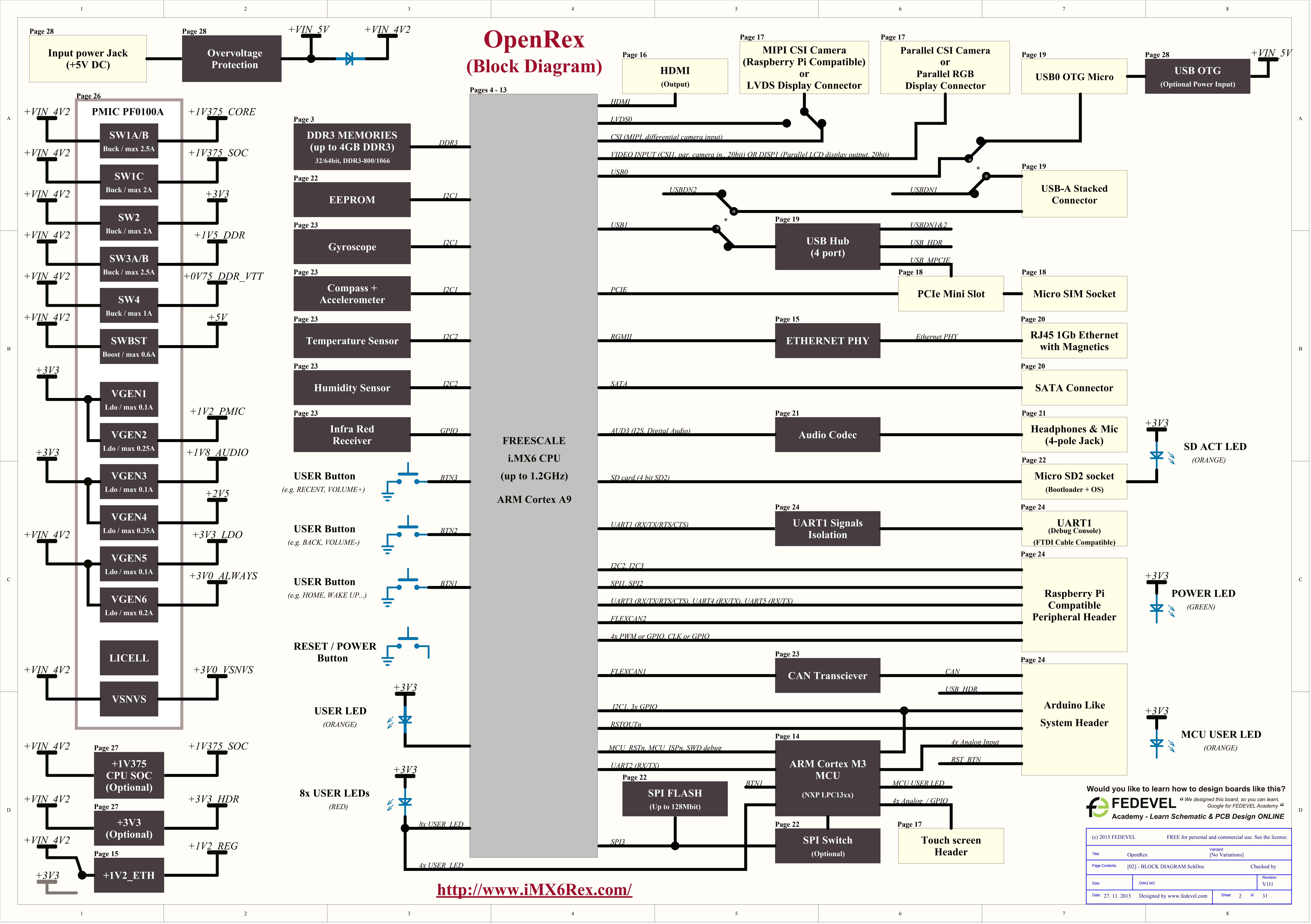


Would you like to learn how to design boards like this?

FEDEVEL *“We designed this board, so you can learn, Google for FEDEVEL Academy“*

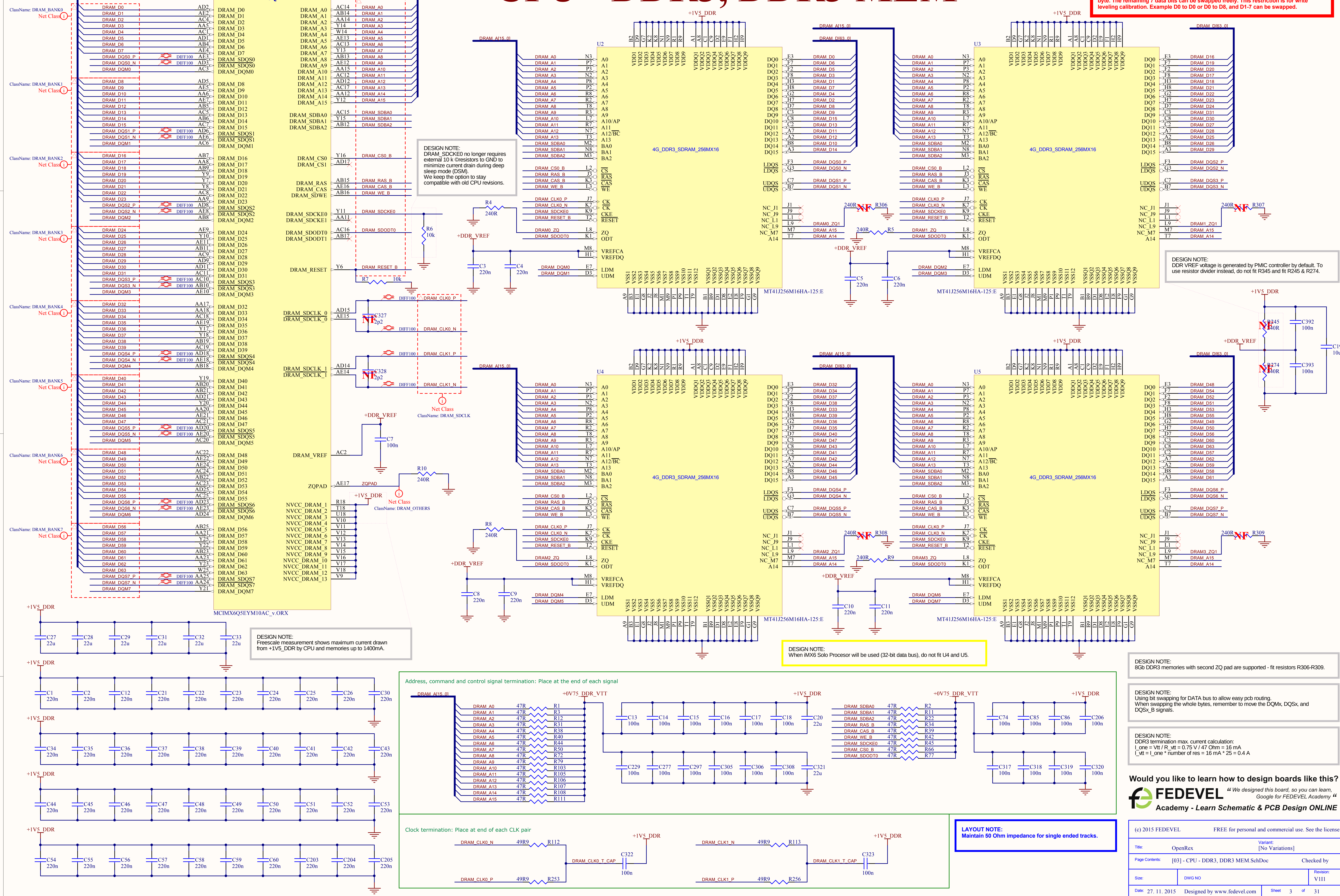
Academy - *Learn Schematic & PCB Design ONLINE*

Title: OpenRex		Variant: [No Variations]	
Page Contents: [01] - COVER PAGE.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 1 of 31	



OpenRex
(Block Diagram)
Page 28
Input power Jack
(+5V DC)
Page 28
Overvoltage
Protection
+VIN_5V
+VIN_4V2
Page 26
PMIC PF0100A
SW1A/B
Buck / max 2.5A
+1V375_CORE
SW1C
Buck / max 2A
+1V375_SOC
SW2
Buck / max 2A
+3V3
SW3A/B
Buck / max 2.5A
+1V5_DDR
SW4
Buck / max 1A
+0V75_DDR_VTT
SWBST
Boost / max 0.6A
+5V
VGEN1
Ldo / max 0.1A
+1V2_PMIC
VGEN2
Ldo / max 0.25A
+1V8_AUDIO
VGEN3
Ldo / max 0.1A
+2V5
VGEN4
Ldo / max 0.35A
+3V3_LDO
VGEN5
Ldo / max 0.1A
+3V0_ALWAYS
VGEN6
Ldo / max 0.2A
LICELL
VSNVS
+3V0_VSNVS
Page 27
+1V375
CPU SOC
(Optional)
Page 27
+3V3
(Optional)
+3V3_HDR
Page 15
+1V2_ETH
+1V2_REG
Page 3
DDR3 MEMORIES
(up to 4GB DDR3)
32/64bit, DDR3-800/1066
DDR3
Page 22
EEPROM
I2C1
Page 23
Gyroscope
Page 23
Compass +
Accelerometer
Page 23
Temperature Sensor
I2C2
Page 23
Humidity Sensor
Page 23
Infra Red
Receiver
GPIO
USER Button
(e.g. RECENT, VOLUME+)
BTN3
USER Button
(e.g. BACK, VOLUME-)
BTN2
USER Button
(e.g. HOME, WAKE UP...)
BTN1
RESET / POWER
Button
USER LED
(ORANGE)
8x USER LEDs
(RED)
8x USER LED
4x USER LED
Pages 4 - 13
FREESCALE
i.MX6 CPU
(up to 1.2GHz)
ARM Cortex A9
Page 16
HDMI
(Output)
Page 17
MIPI CSI Camera
(Raspberry Pi Compatible)
or
LVDS Display Connector
Page 17
Parallel CSI Camera
or
Parallel RGB
Display Connector
Page 19
USB0 OTG Micro
Page 28
USB OTG
(Optional Power Input)
HDMI
LVDS0
CSI (MIPI, differential camera input)
VIDEO INPUT (CSI1, par. camera in., 20bit) OR DISP1 (Parallel LCD display output, 20bit)
USB0
USBDN2
USBDN1
Page 19
USB-A Stacked
Connector
USB1
Page 19
USB Hub
(4 port)
USBDN1&2
USB_HDR
USB_MPCIE
Page 18
PCIe Mini Slot
Page 18
Micro SIM Socket
PCIE
Page 15
ETHERNET PHY
RGMII
Ethernet PHY
Page 20
RJ45 1Gb Ethernet
with Magnetics
Page 20
SATA Connector
SATA
Page 21
Audio Codec
AUD3 (I2S, Digital Audio)
Page 21
Headphones & Mic
(4-pole Jack)
Page 22
Micro SD2 socket
(Bootloader + OS)
SD card (4 bit SD2)
SD ACT LED
(ORANGE)
Page 24
UART1 Signals
Isolation
UART1 (RX/TX/RTS/CTS)
Page 24
UART1
(Debug Console)
(FTDI Cable Compatible)
Page 24
I2C2, I2C3
SPI1, SPI2
UART3 (RX/TX/RTS/CTS), UART4 (RX/TX), UART5 (RX/TX)
FLEXCAN2
4x PWM or GPIO, CLK or GPIO
Raspberry Pi
Compatible
Peripheral Header
POWER LED
(GREEN)
Page 23
CAN Transciever
FLEXCAN1
CAN
USB_HDR
Page 24
Arduino Like
System Header
I2C1, 3x GPIO
RSTOUTn
MCU_RSTn, MCU_ISPn, SWD debug
UART2 (RX/TX)
4x Analog Input
RST_BTN
Page 14
ARM Cortex M3
MCU
(NXP LPC13xx)
MCU USER LED
(ORANGE)
MCU USER LED
4x Analog / GPIO
BTN1
Page 22
SPI FLASH
(Up to 128Mbit)
SPI3
Page 22
SPI Switch
(Optional)
Page 17
Touch screen
Header
http://www.iMX6Rex.com/
Would you like to learn how to design boards like this?
FEDEVEL
"We designed this board, so you can learn, Google for FEDEVEL Academy"
Academy - Learn Schematic & PCB Design ONLINE
(c) 2015 FEDEVEL
FREE for personal and commercial use. See the license.
Title: OpenRex
Variant: [No Variations]
Page Contents: [02] - BLOCK DIAGRAM.SchDoc
Checked by
Revision: V1I1
Date: 27. 11. 2015
Designed by www.fedevel.com
Sheet 2 of 31

CPU - DDR3, DDR3 MEM



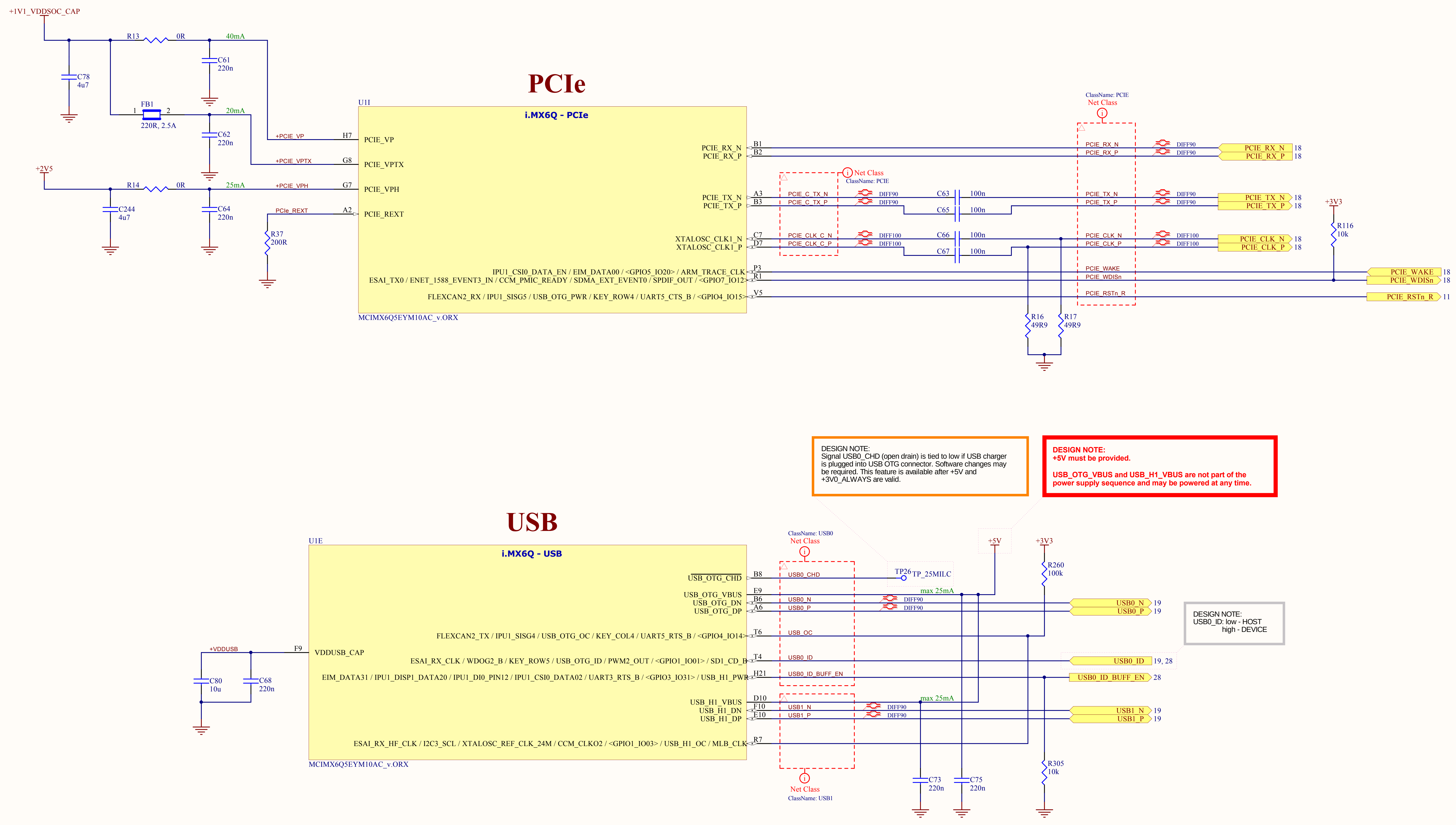
Would you like to learn how to design boards like this?

FEDEVEL Academy - Learn Schematic & PCB Design ONLINE

"We designed this board, so you can learn, Google for FEDEVEL Academy"

Title:	OpenRex
Variant:	[No Variations]
Page Contents:	[03] - CPU - DDR3, DDR3 MEM.SchDoc
Checked by	
Size:	
DWG NO	
Revision:	V1I1
Date:	27. 11. 2015
Designed by	www.fedevel.com
Sheet	3 of 31

CPU - PCIE, USB



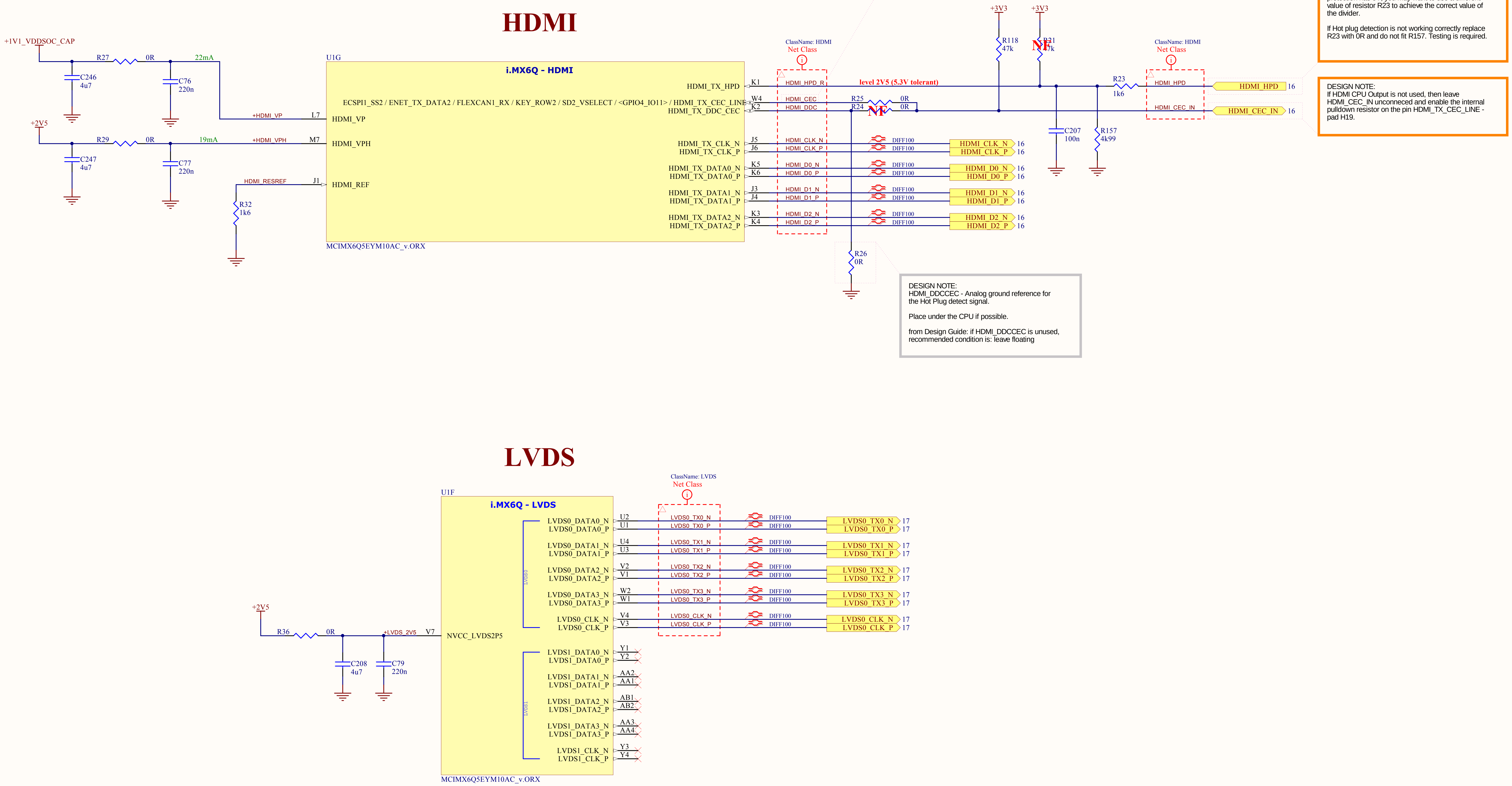
Would you like to learn how to design boards like this?

FEDEVEL "We designed this board, so you can learn, Google for FEDEVEL Academy"

Academy - Learn Schematic & PCB Design ONLINE

Title: OpenRex		Variant: [No Variations]	
Page Contents: [04] - CPU - PCIE, USB.SchDoc		Checked by	
Size:	DWG NO	Revision: V1I1	
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 4 of 31	

CPU - HDMI, LVDS

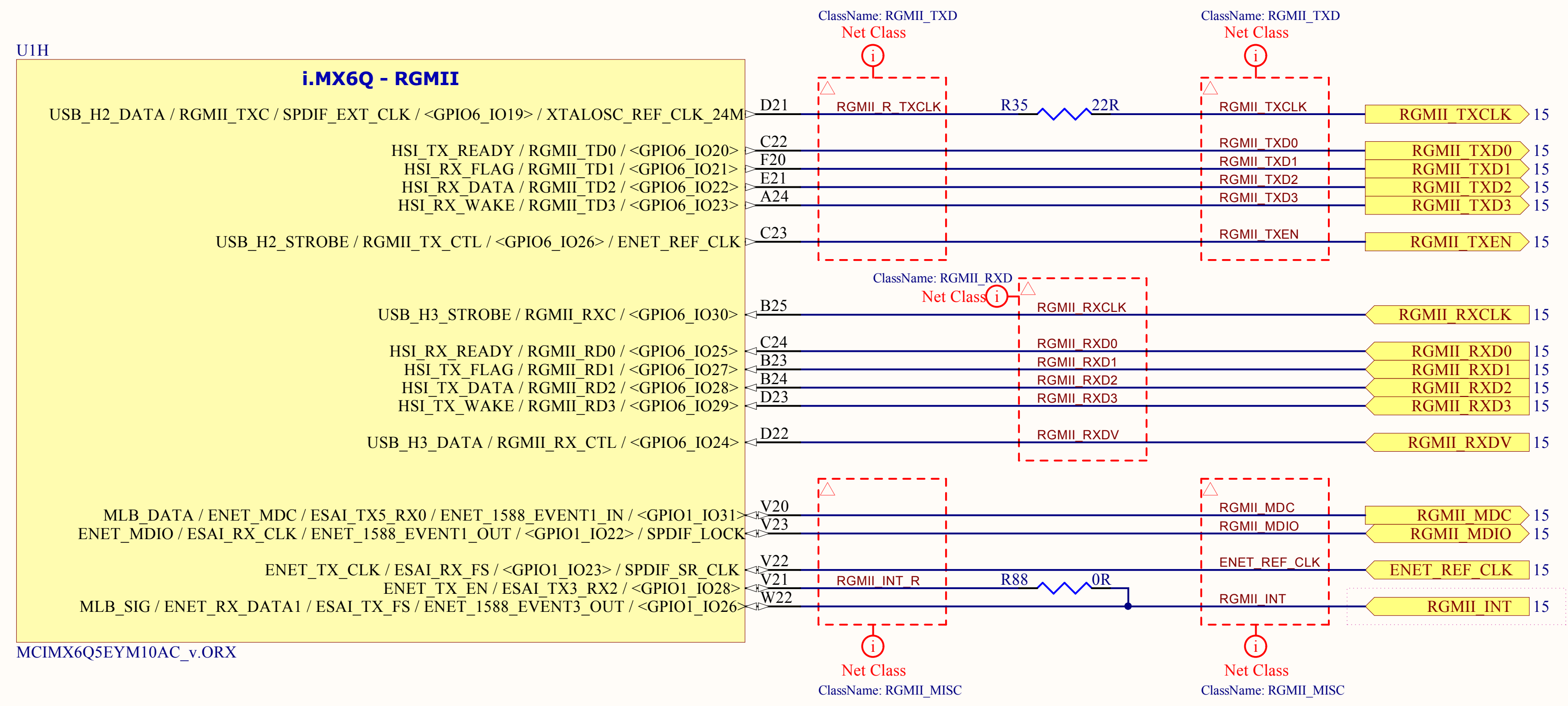


Would you like to learn how to design boards like this?
FEDEVEL Academy - Learn Schematic & PCB Design ONLINE
"We designed this board, so you can learn, Google for FEDEVEL Academy"

Title: OpenRex	Variant: [No Variations]
Page Contents: [05] - CPU - HDMI, LVDS.SchDoc	Checked by
Size:	DWG NO	Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 5 of 31

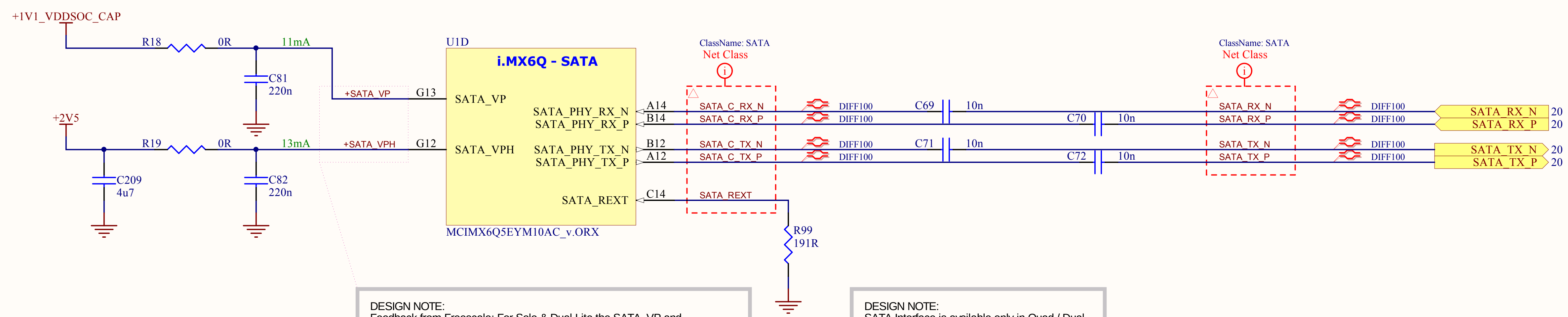
CPU - ETHERNET, SATA

ETHERNET



DESIGN NOTE:
If there is a problem with RGMII Interrupt, unfit R88.

SATA



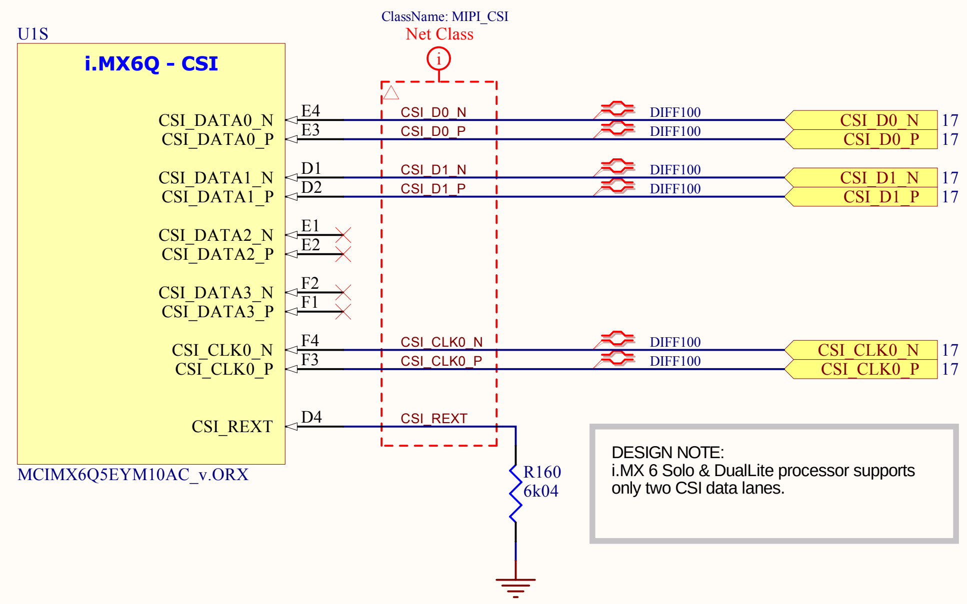
DESIGN NOTE:
Feedback from Freescale: For Solo & Dual Lite the SATA_VP and SATA_VPH pins should be powered if performing boundary scan tests.

DESIGN NOTE:
SATA Interface is available only in Quad / Dual version of i.MX6 processor.

Title: OpenRex		Variant: [No Variations]	
Page Contents: [06] - CPU - ETHERNET, SATA.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 6 of 31	

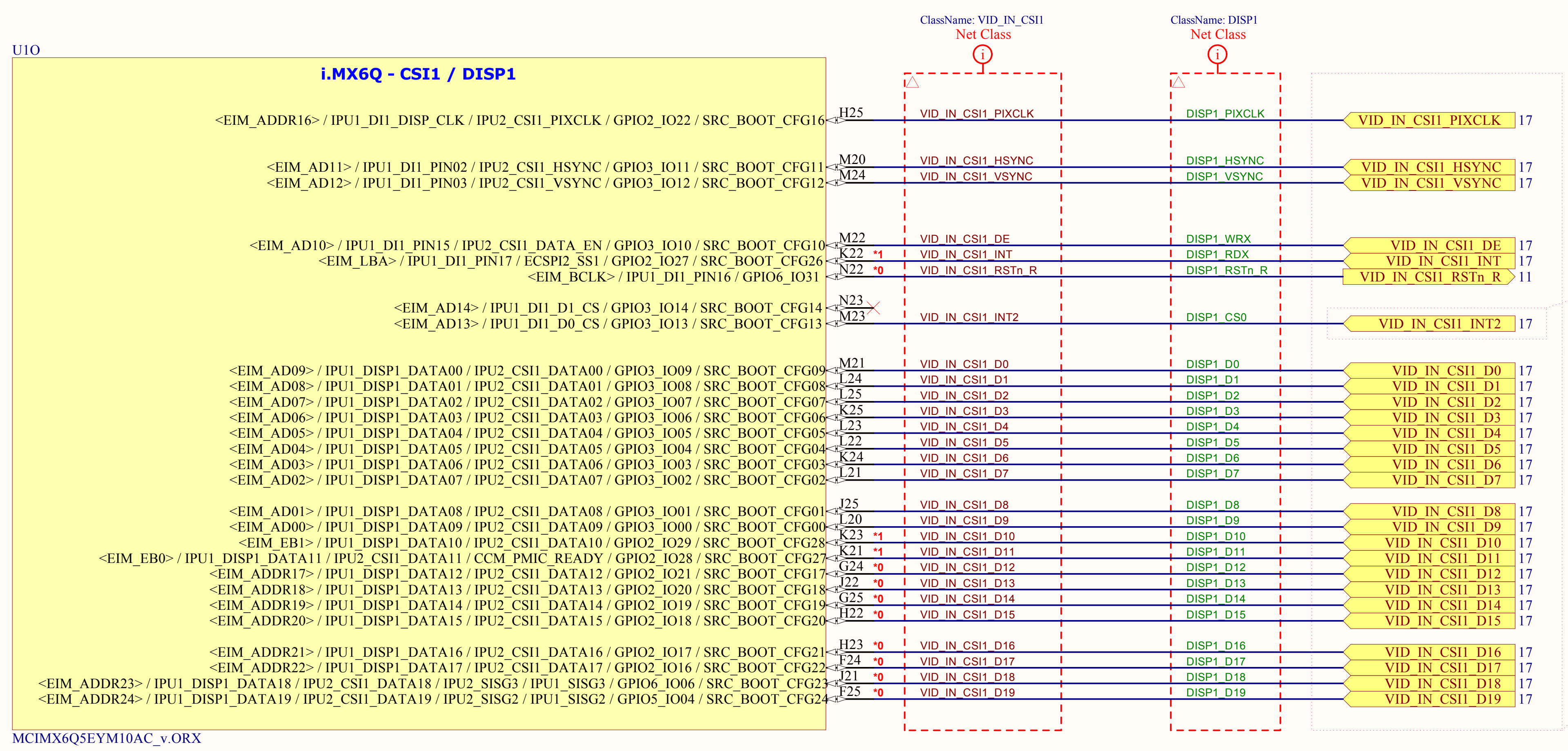
CPU - CSI, DISP

Serial Camera Interface CSI



DESIGN NOTE:
i.MX 6 Solo & DualLite processor supports only two CSI data lanes.

Parallel Camera Interface CSI1 / DISP1



DESIGN NOTE:
Use VID_IN_CSI1_INT2 also to detect a connected camera module. Set internall pull down resistor for VID_IN_CSI1_INT2 and place an external 3k3 pull up on the camera module. When a camera module is connected, software can detect High level on VID_IN_CSI1_INT2 pin.

DESIGN NOTE:
Parallel camera interface CSI1 signals can be also used as DISP1 Interface .

DESIGN NOTE:
Be aware, after reset some CSI1 / DISP1 pins are set as outputs. Be sure before you enable a camera, these pins should be set correctly as inputs otherwise there may be a conflict between camera and CPU pins.

Default state of CSI1/DISP1 signal after reset:
***0 - Ouptut Low**
***1 - Output High**
without mark - 100k pullup to +3V3

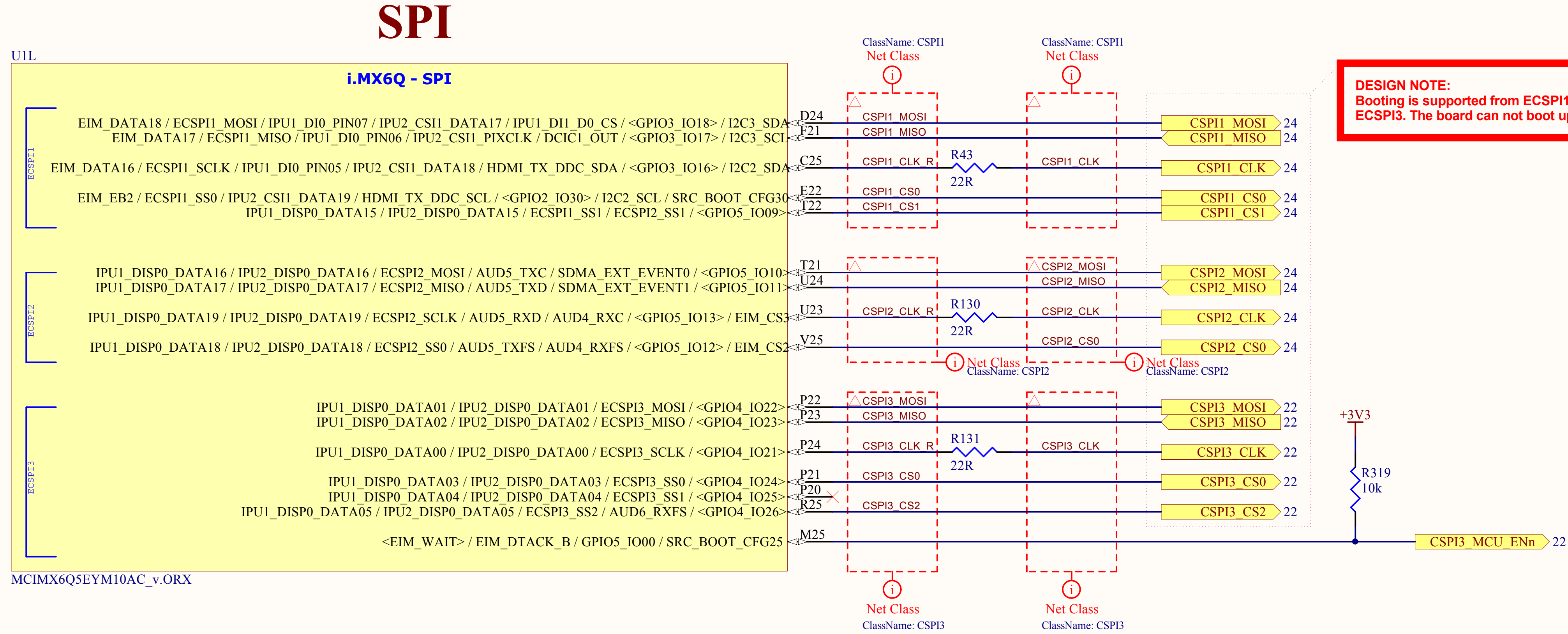
DESIGN NOTE:
Supported CAMERA modes: 8bit RGB 565 / 666 / 888, 16bit RGB565, 8/16/20bit YCbCr. See more information about pin mapping in IMX6DQAEC.pdf (Table 66. Camera Input Signal Cross Reference, Format, and Bits Per Cycle).

DESIGN NOTE:
Supported DISPLAY modes: 16/18bit RGB, 8/16/20bit YCrCb. See more information about pin mapping in IMX6DQAEC.pdf (Table 68. Video Signal Cross-Reference).

Title: OpenRex		Variant: [No Variations]	
Page Contents: [07] - CPU - CSI, DISP.SchDoc		Checked by	
Size:	DWG NO	Revision: V1I1	
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 7 of 31	

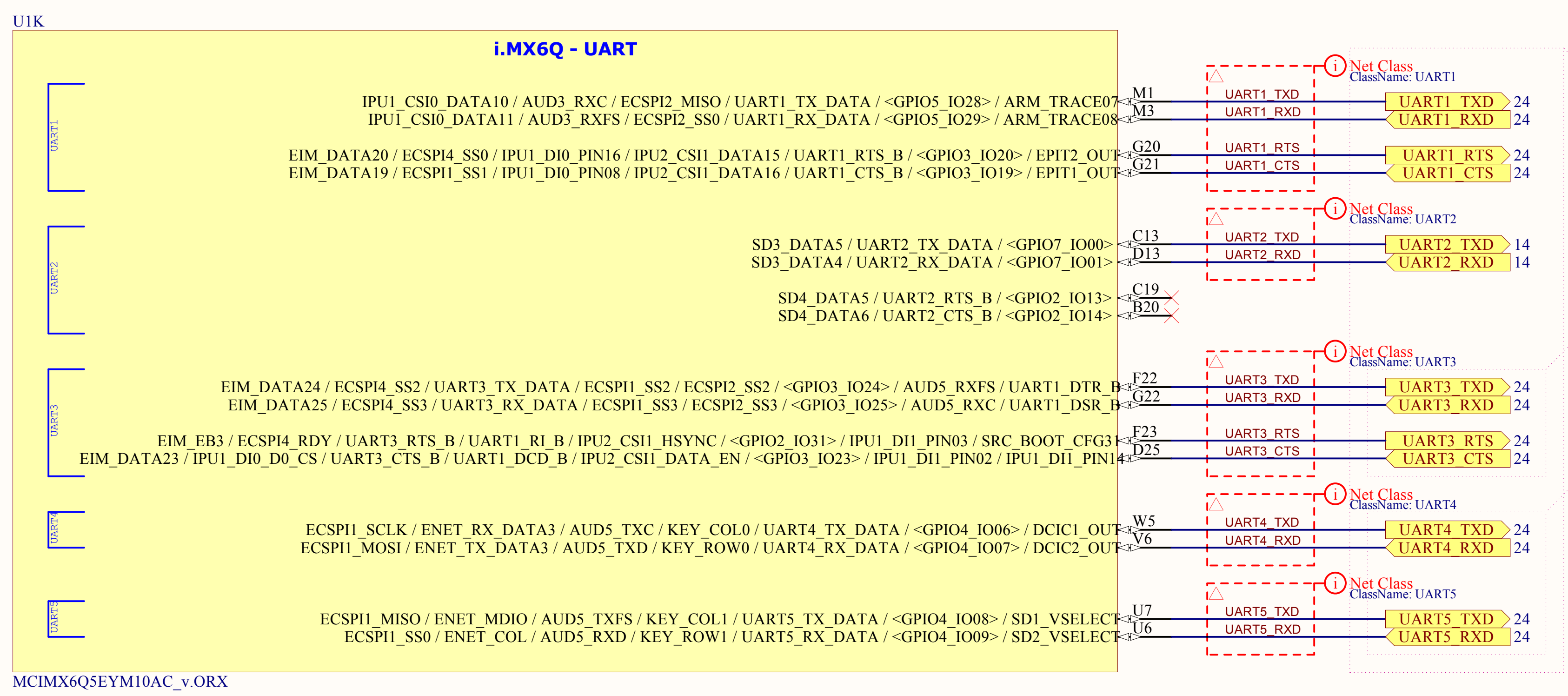
CPU - SPI, UART

SPI



DESIGN NOTE:
Booting is supported from ECSPI1 (CS0 only) and ECSPI3. The board can not boot up from ECSPI2.

UART



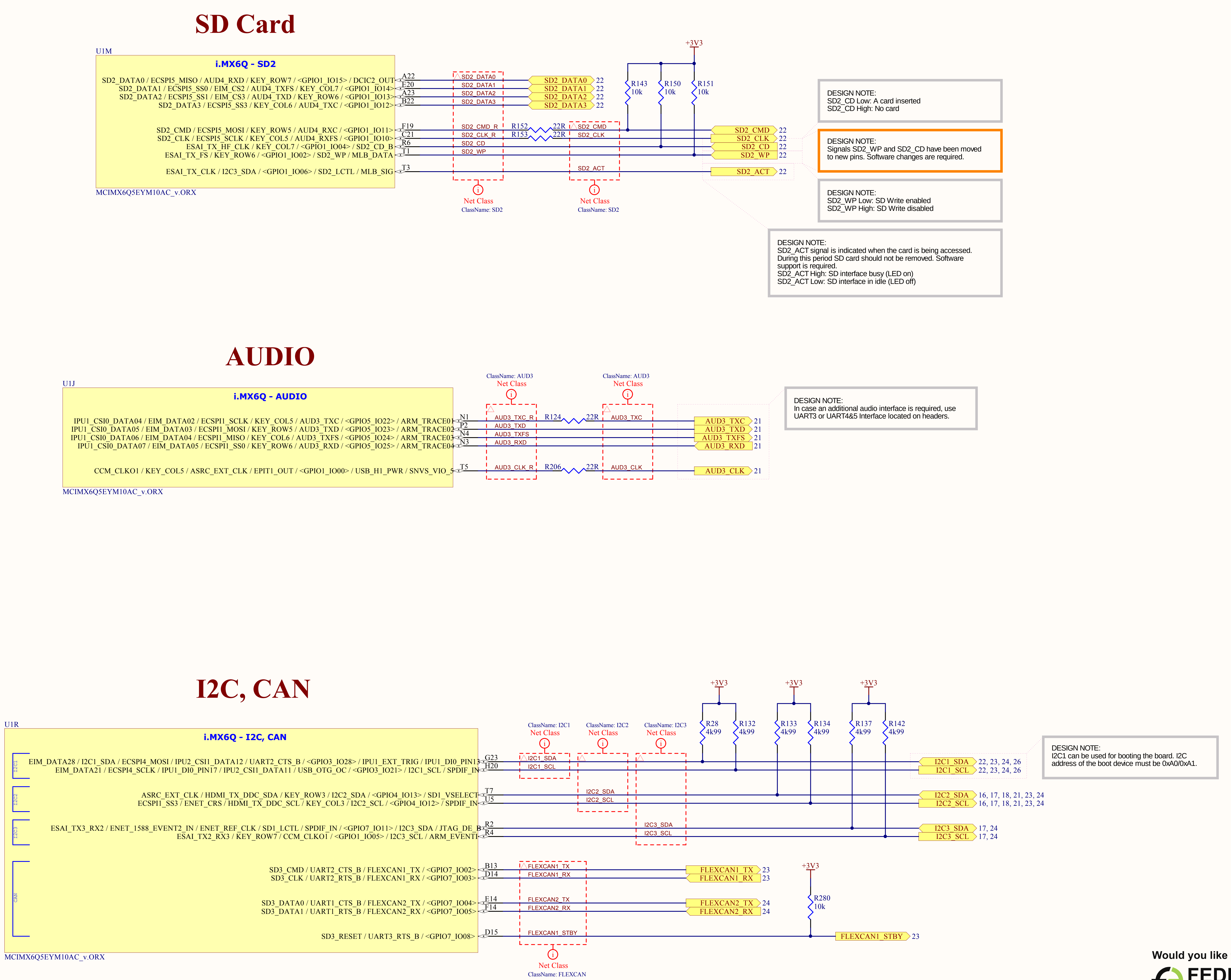
DESIGN NOTE:
All UART signals should be configured in software (except UART1_TXD & UART1_RXD.

DESIGN NOTE:
UART3 signals can be used for full UART1 Interface or as another audio I2S interface on header.

DESIGN NOTE:
UART 4 & 5 can be grouped as an additional audio interface (external clock may be required).

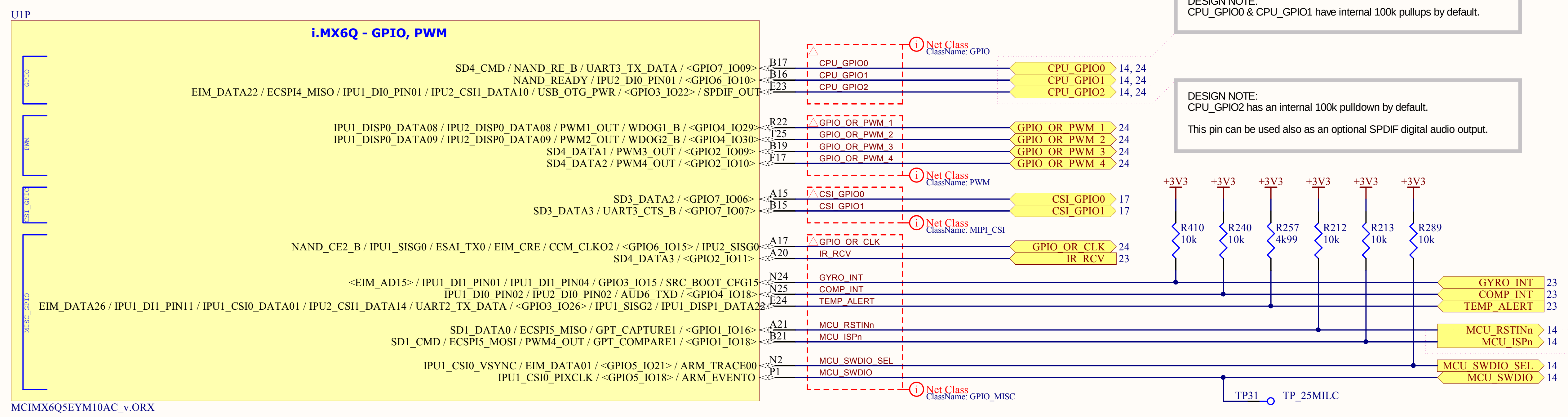
Title: OpenRex		Variant: [No Variations]	
Page Contents: [08] - CPU - SPI, UART.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 8 of 31	

CPU - SD CARD, AUDIO, I2C, CAN



CPU - GPIO, PWM, LEDS, BUTTONS

GPIO, PWM



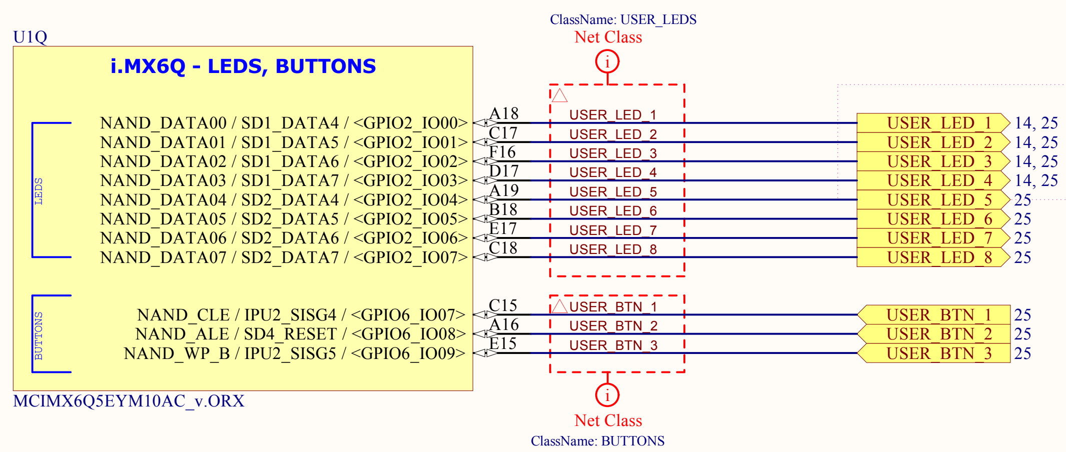
DESIGN NOTE:
CPU_GPIO0 & CPU_GPIO1 have internal 100k pullups by default.

DESIGN NOTE:
CPU_GPIO2 has an internal 100k pulldown by default.

This pin can be used also as an optional SPDIF digital audio output.

DESIGN NOTE:
Setup MCU_ISPn CPU pin as an open drain, when it is not used during the MCU programming.

LEDS, BUTTONS



DESIGN NOTE:
Set LEDs as open collector outputs (possible with pullup resistors) to avoid conflict with microcontroller pins.

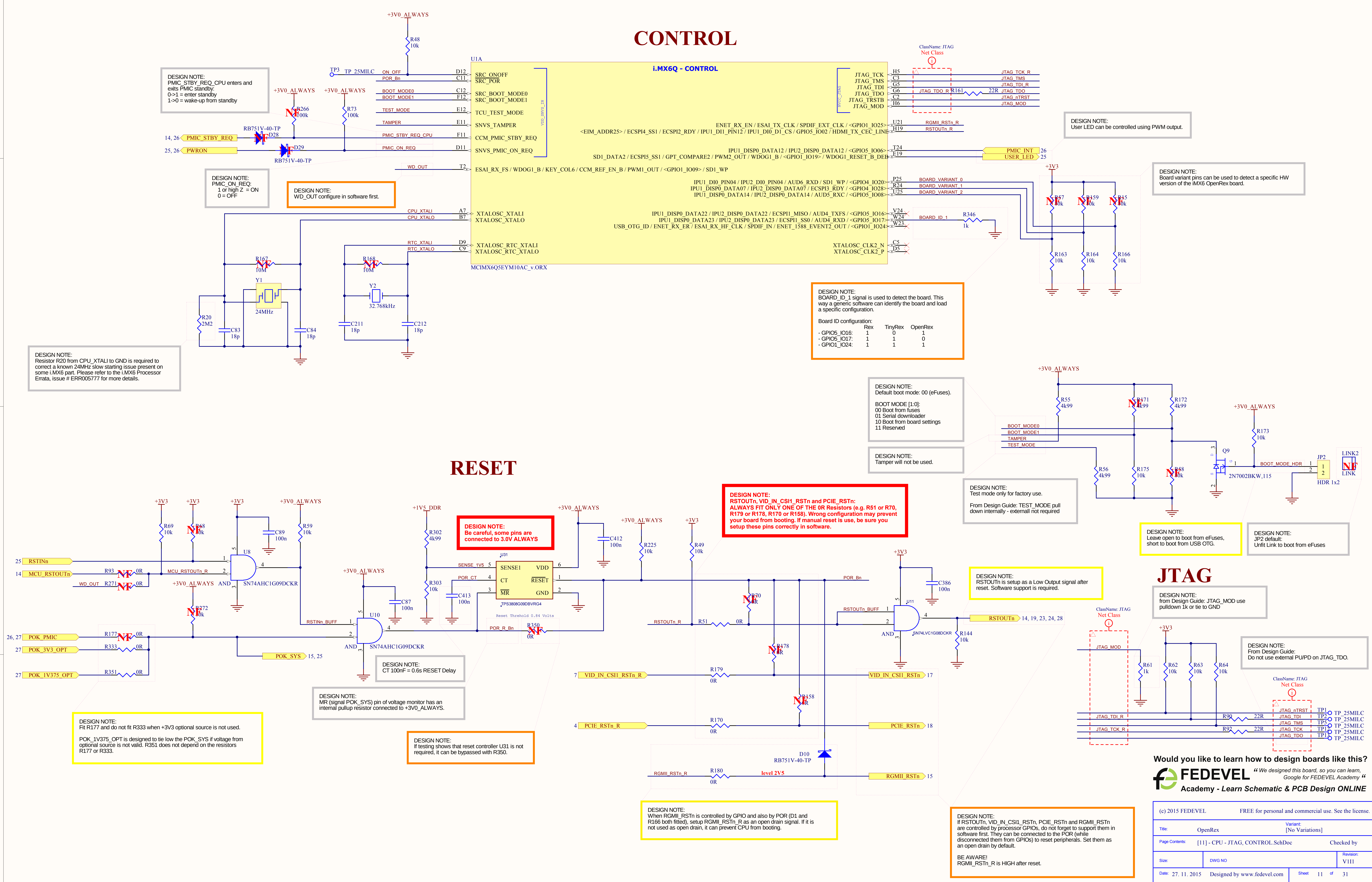
Would you like to learn how to design boards like this?

FEDEVEL *" We designed this board, so you can learn, Google for FEDEVEL Academy "*

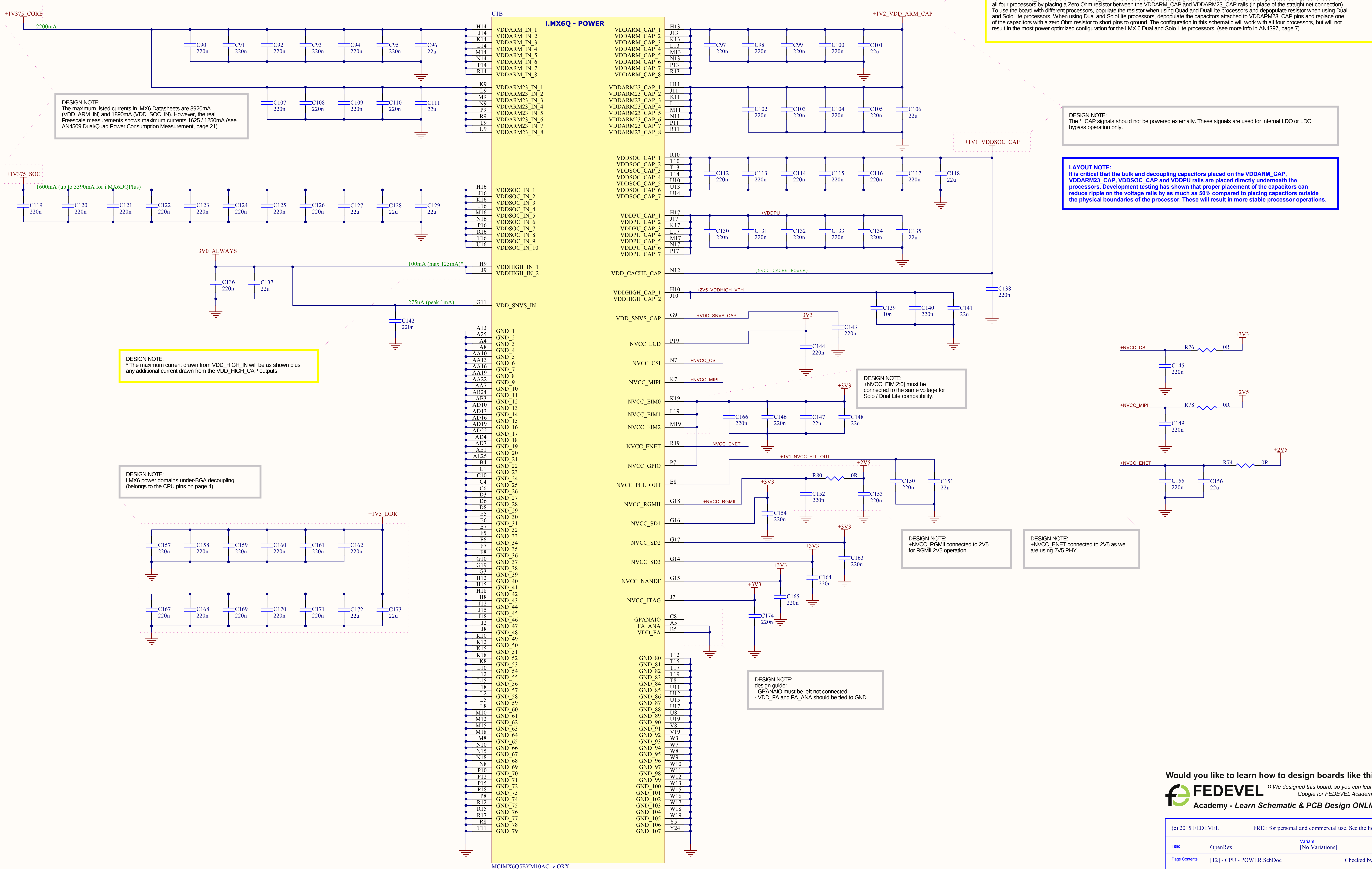
Academy - *Learn Schematic & PCB Design ONLINE*

Title: OpenRex		Variant: [No Variations]	
Page Contents: [10] - CPU - GPIO, PWM, LEDS, BUTTONS.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 10 of 31	

CPU - JTAG, CONTROL



CPU - POWER



DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo Lite processors. (see more info in AN4397, page 7)

DESIGN NOTE:
The maximum listed currents in iMX6 Datasheets are 3920mA (VDD_ARM_IN) and 1890mA (VDD_SOC_IN). However, the real Freescale measurements shows maximum currents 1625 / 1250mA (see AN4509 Dual/Quad Power Consumption Measurement, page 21)

DESIGN NOTE:
The *_CAP signals should not be powered externally. These signals are used for internal LDO or LDO bypass operation only.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails are placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

DESIGN NOTE:
* The maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs.

DESIGN NOTE:
+NVCC_EIM[2:0] must be connected to the same voltage for Solo / Dual Lite compatibility.

DESIGN NOTE:
i.MX6 power domains under-BGA decoupling (belongs to the CPU pins on page 4).

DESIGN NOTE:
+NVCC_RGMII connected to 2V5 for RGMII 2V5 operation.

DESIGN NOTE:
+NVCC_ENET connected to 2V5 as we are using 2V5 PHY.

DESIGN NOTE:
design guide:
- GPANAIO must be left not connected
- VDD_FA and FA_ANA should be tied to GND.

Would you like to learn how to design boards like this?

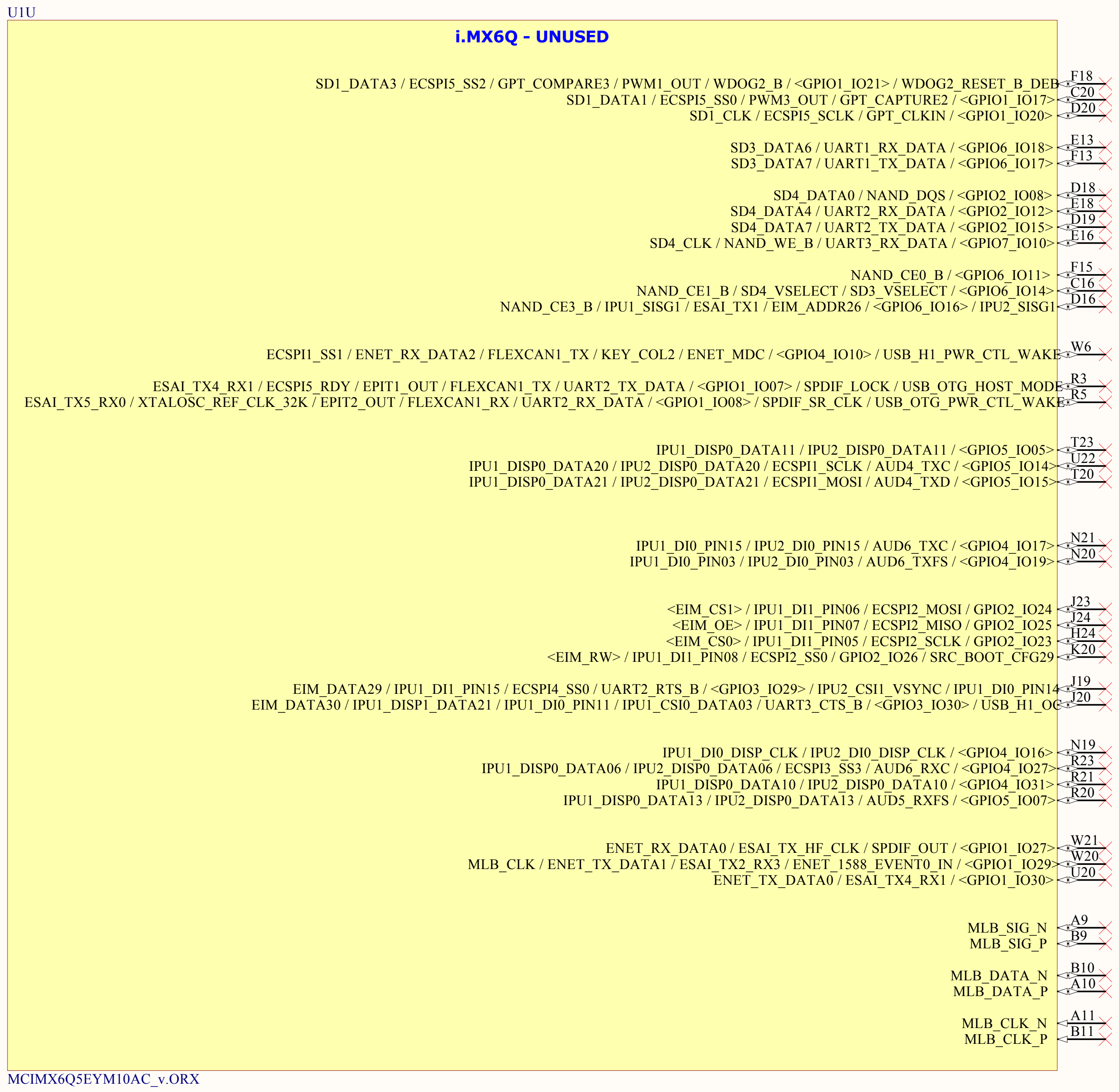
FEDEVEL “We designed this board, so you can learn, Google for FEDEVEL Academy”

Academy - Learn Schematic & PCB Design ONLINE

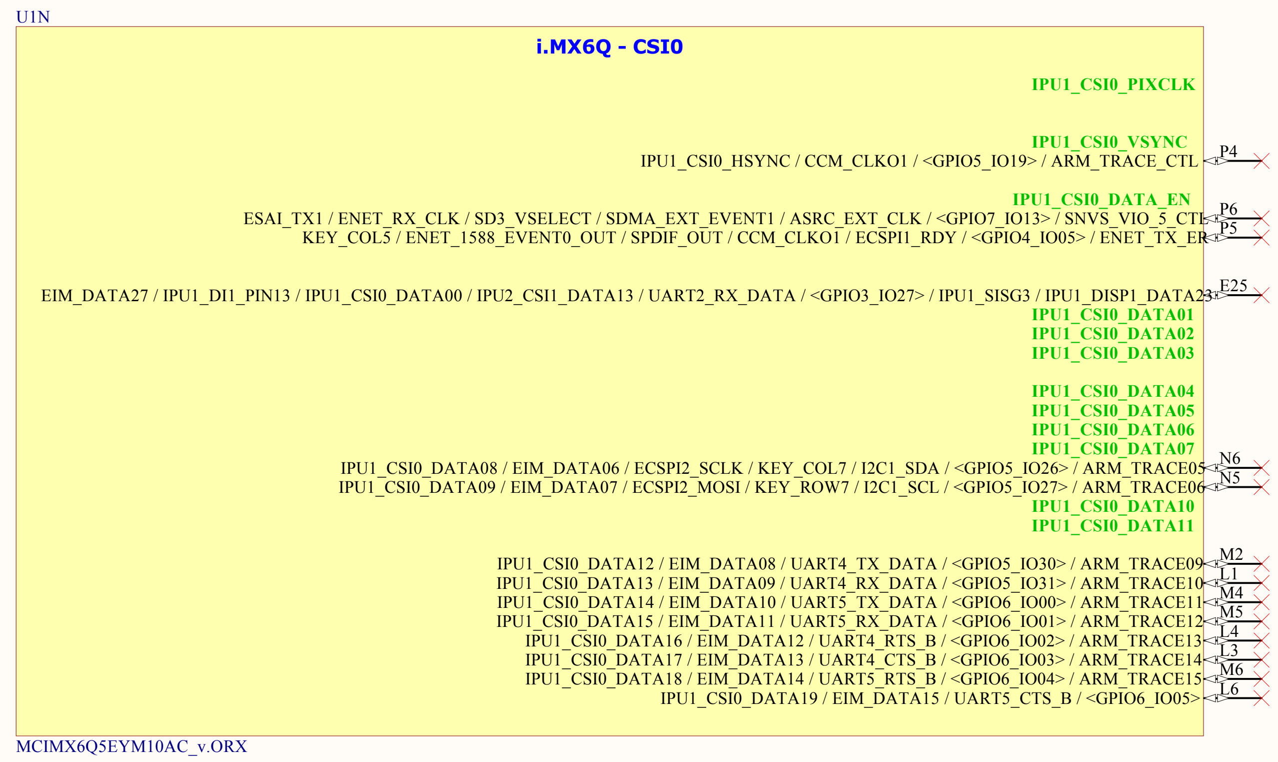
Title: OpenRex	Variant: [No Variations]
Page Contents: [12] - CPU - POWER.SchDoc	Checked by
Size: DWG NO	Revision: V1I1
Date: 27. 11. 2015 Designed by www.fedevel.com	Sheet 12 of 31

CPU - UNUSED PINS

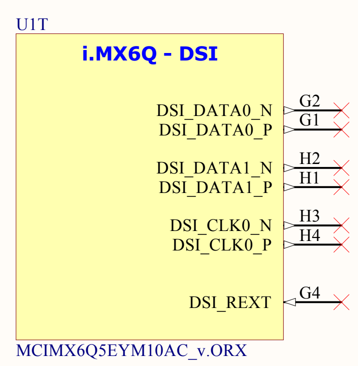
MISC



Parallel Camera Interface CSI0

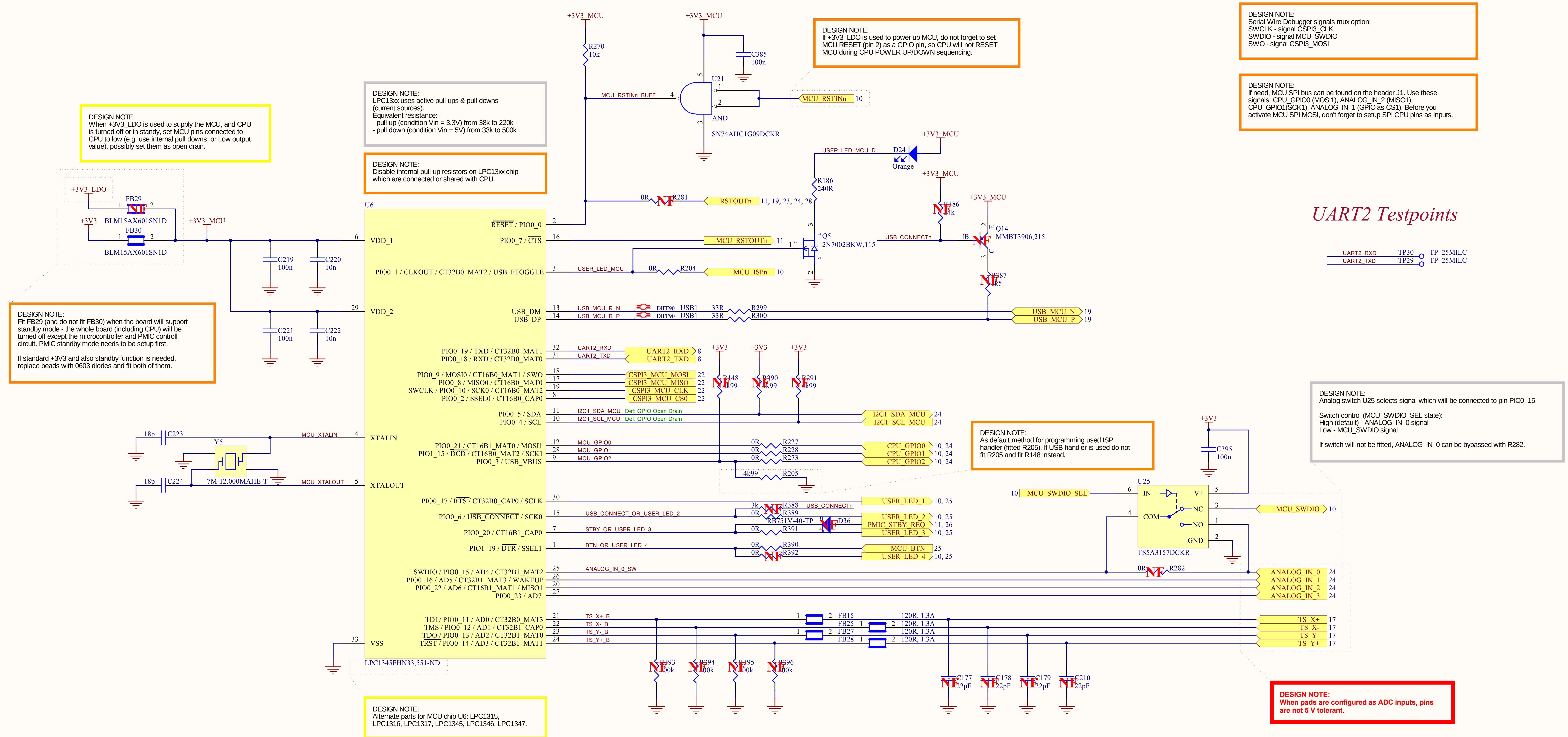


Serial Display Interface DSI



Title: OpenRex
Variant: [No Variations]
Page Contents: [13] - CPU - UNUSED.SchDoc
Checked by
Size:
DWG NO
Revision: V1I1
Date: 27. 11. 2015 Designed by www.fedevel.com

MCU



DESIGN NOTE:
When +3V3_LDO is used to supply the MCU, and CPU is turned off or in standy, set MCU pins connected to CPU to low (e.g. use internal pull downs, or Low output value), possibly set them as open drain.

DESIGN NOTE:
LPC13xx uses active pull ups & pull downs (current sources).
Equivalent resistance:
- pull up (condition Vin = 3.3V) from 38k to 220k
- pull down (condition Vin = 5V) from 33k to 500k

DESIGN NOTE:
Disable internal pull up resistors on LPC13xx chip which are connected or shared with CPU.

DESIGN NOTE:
If +3V3_LDO is used to power up MCU, do not forget to set MCU RESET (pin 2) as a GPIO pin, so CPU will not reset MCU during CPU POWER UP/DOWN sequencing.

DESIGN NOTE:
Serial Wire Debugger signals mux option:
SWCLK - signal CSPI3_CLK
SWDIO - signal MCU_SWDIO
SWO - signal CSPI3_MOSI

DESIGN NOTE:
If need, MCU SPI bus can be found on the header J1. Use these signals: CPU_GPIO0 (MOSI1), ANALOG_IN_2 (MISO1), CPU_GPIO1(SCK1), ANALOG_IN_1 (GPIO as CS1). Before you activate MCU SPI MOSI, don't forget to setup SPI CPU pins as inputs.

UART2 Testpoints

UART2_RXD TP30 TP_25MILC
UART2_TXD TP29 TP_25MILC

DESIGN NOTE:
Fit FB29 (and do not fit FB30) when the board will support standby mode - the whole board (including CPU) will be turned off except the microcontroller and PMIC controll circuit. PMIC standby mode needs to be setup first.

If standard +3V3 and also standby function is needed, replace beads with 0603 diodes and fit both of them.

DESIGN NOTE:
As default method for programming used ISP handler (fitted R205). If USB handler is used do not fit R205 and fit R148 instead.

DESIGN NOTE:
Analog switch U25 selects signal which will be connected to pin PIO0_15.

Switch control (MCU_SWDIO_SEL state):
High (default) - ANALOG_IN_0 signal
Low - MCU_SWDIO signal

If switch will not be fitted, ANALOG_IN_0 can be bypassed with R282.

DESIGN NOTE:
When pads are configured as ADC inputs, pins are not 5 V tolerant.

DESIGN NOTE:
Alternate parts for MCU chip U6: LPC1315, LPC1316, LPC1317, LPC1345, LPC1346, LPC1347.

Title: OpenRex		Variant: [No Variations]	
Page Contents: [14] - MCU.SchDoc		Checked by	
Size:	DWG NO	Revision: V1I1	
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 14 of 31	

ETHERNET PHY

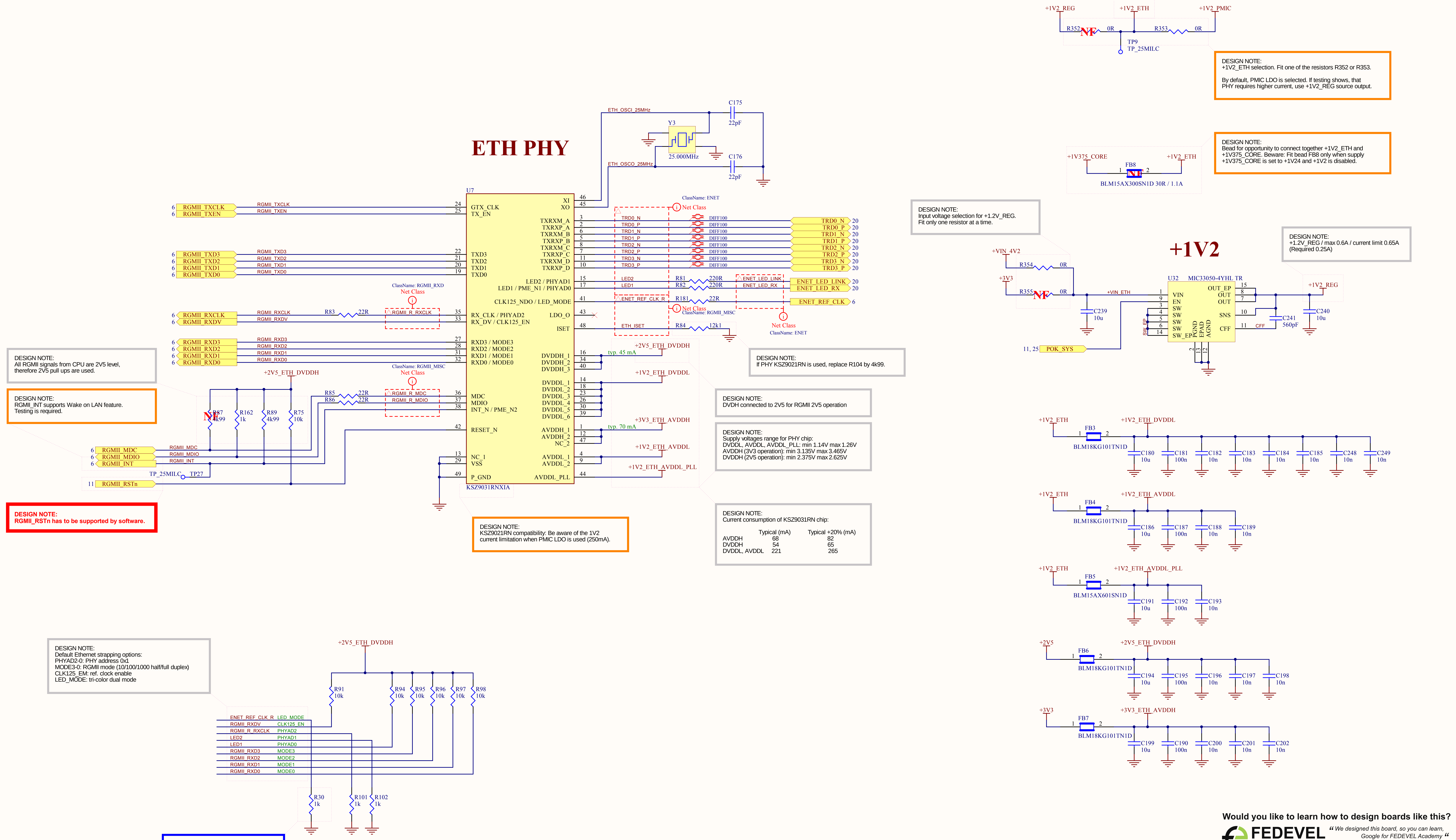
DESIGN NOTE:
+1V2_ETH power rail
+1.2V / Required 250mA

DESIGN NOTE:
+1V2_ETH selection. Fit one of the resistors R352 or R353.

By default, PMIC LDO is selected. If testing shows, that PHY requires higher current, use +1V2_REG source output.

DESIGN NOTE:
Bead for opportunity to connect together +1V2_ETH and +1V375_CORE. Beware: Fit bead FB8 only when supply +1V375_CORE is set to +1V24 and +1V2 is disabled.

ETH PHY



DESIGN NOTE:
Input voltage selection for +1.2V_REG.
Fit only one resistor at a time.

DESIGN NOTE:
+1.2V_REG / max 0.6A / current limit 0.65A
(Required 0.25A)

DESIGN NOTE:
All RGMII signals from CPU are 2V5 level, therefore 2V5 pull ups are used.

DESIGN NOTE:
RGMII_INT supports Wake on LAN feature.
Testing is required.

DESIGN NOTE:
If PHY KSZ9021RN is used, replace R104 by 4k99.

DESIGN NOTE:
DVDH connected to 2V5 for RGMII 2V5 operation

DESIGN NOTE:
Supply voltages range for PHY chip:
DVDDL, AVDDL, AVDDL_PLL: min 1.14V max 1.26V
AVDDH (3V3 operation): min 3.135V max 3.465V
DVDDH (2V5 operation): min 2.375V max 2.625V

DESIGN NOTE:
RGMII_RSTn has to be supported by software.

DESIGN NOTE:
KSZ9021RN compatibility: Be aware of the 1V2 current limitation when PMIC LDO is used (250mA).

DESIGN NOTE:
Current consumption of KSZ9031RN chip:

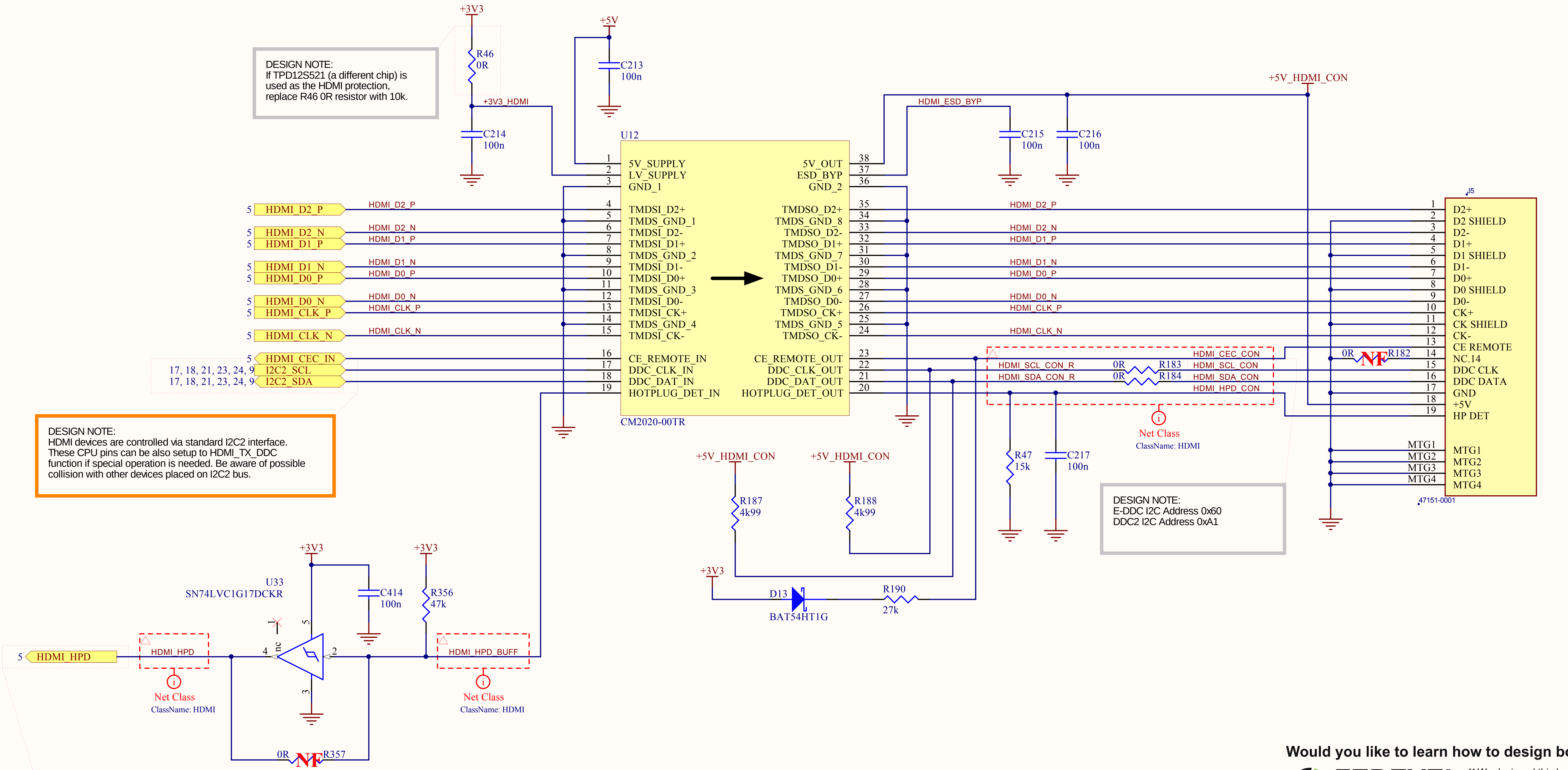
	Typical (mA)	Typical +20% (mA)
AVDDH	68	82
DVDDH	54	65
DVDDL, AVDDL	221	265

DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2-0: PHY address 0x1
MODE3-0: RGMII mode (10/100/1000 half/full duplex)
CLK125_EN: ref. clock enable
LED_MODE: tri-color dual mode

LAYOUT NOTE:
Be sure you place R30 directly on the net to minimize stubs.

Title: OpenRex
Variant: [No Variations]
Page Contents: [15] - ETHERNET PHY.SchDoc
Checked by
Size:
DWG NO
Revision: V1I1
Date: 27. 11. 2015 Designed by www.fedevel.com

HDMI Connector



DESIGN NOTE:
If TPD12S521 (a different chip) is used as the HDMI protection, replace R46 0R resistor with 10k.

DESIGN NOTE:
HDMI devices are controlled via standard I2C2 interface. These CPU pins can be also setup to HDMI_TX_DDC function if special operation is needed. Be aware of possible collision with other devices placed on I2C2 bus.

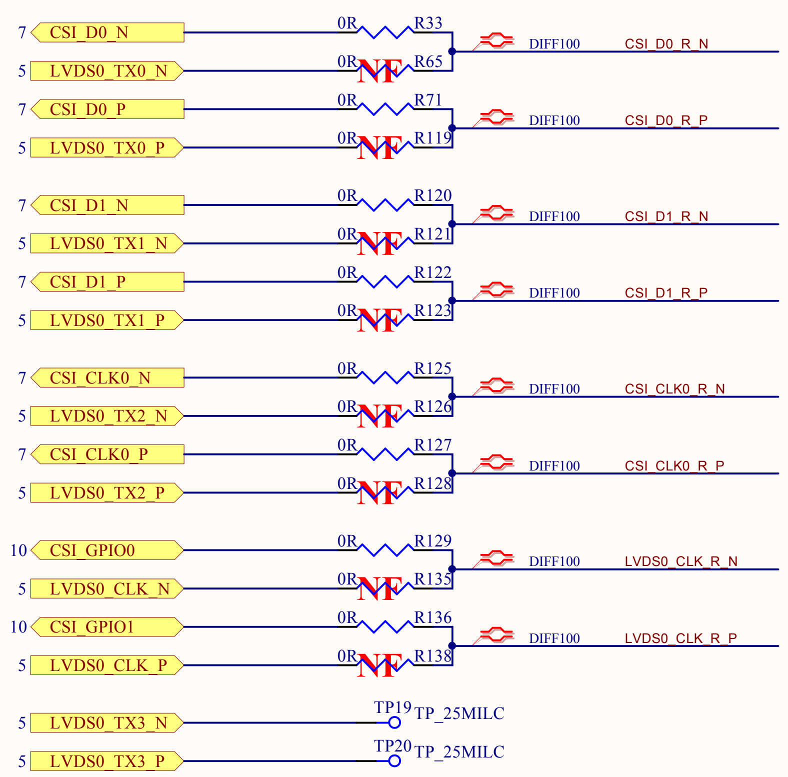
DESIGN NOTE:
E-DDC I2C Address 0x60
DDC2 I2C Address 0xA1

DESIGN NOTE:
From CM2020 datasheet, the HOTPLUG_DET_IN pin specification is not clear. A schmitt buffer is added and after testing can be bypassed by R357.

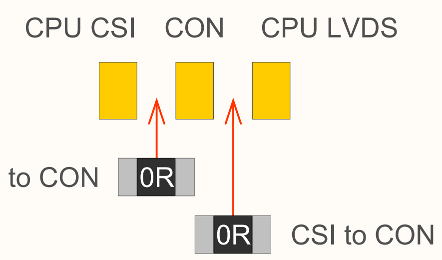
Title: OpenRex		Variant: [No Variations]	
Page Contents: [16] - HDMI.SchDoc		Checked by	
Size:	DWG NO		Revision: V1II
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 16 of 31	

LVDS / CSI, LCD / CSI1 CONNECTORS, TOUSCHSCREEN

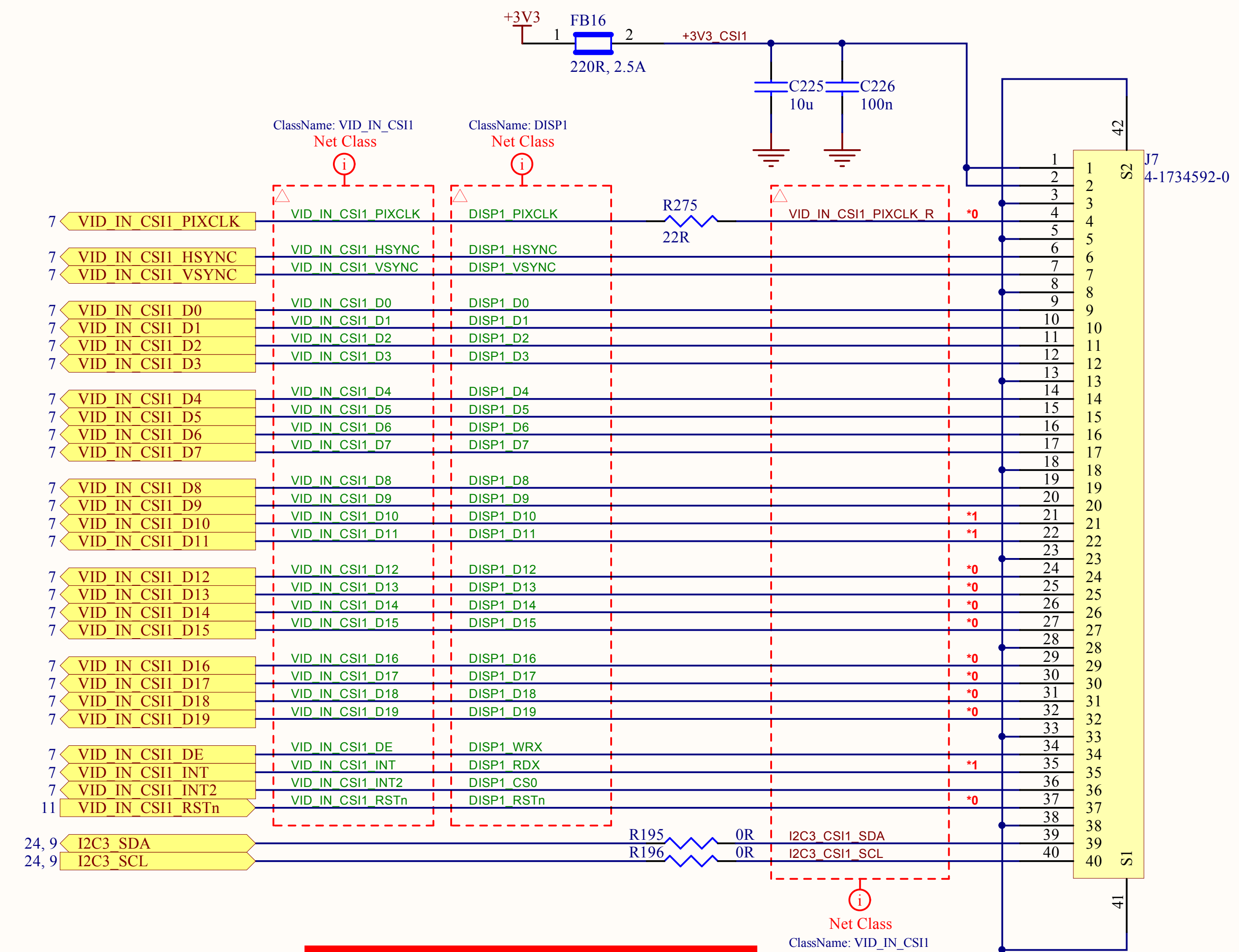
CSI / LVDS Routing



DESIGN NOTE:
Fit only one resistor per one signal according to the picture below.



CSI1 / DISP1 Connector



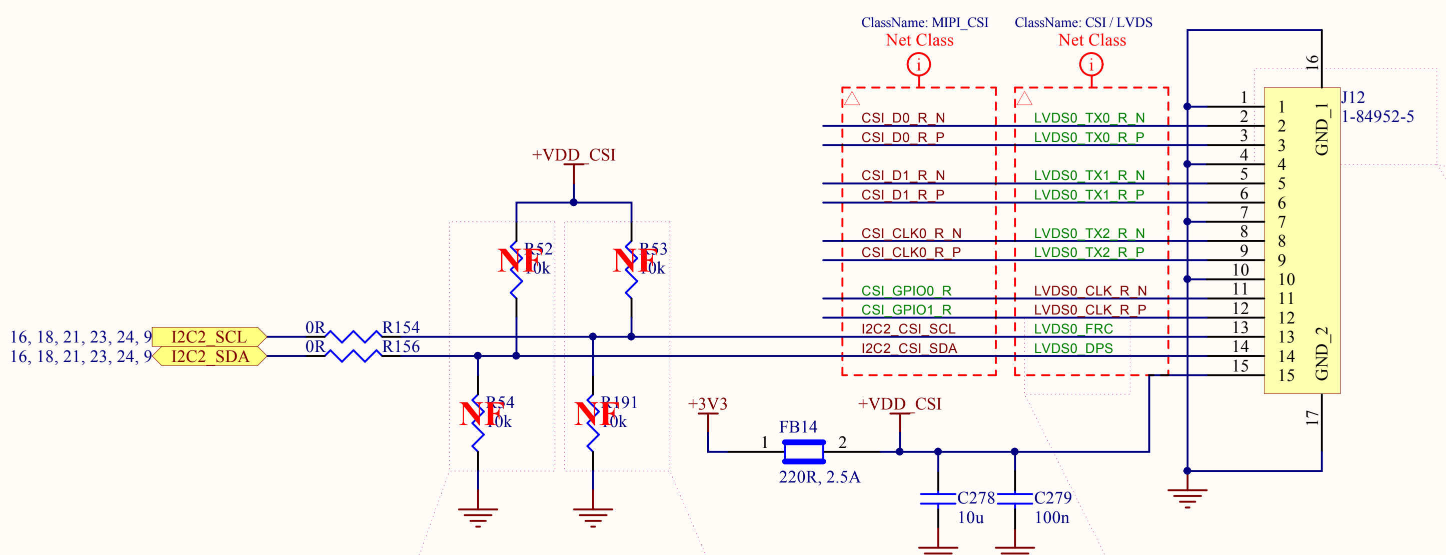
DESIGN NOTE:
Be aware, after reset some CSI1 / DISP1 pins are set as output. Be sure before you enable a camera, these pins should be set correctly as inputs otherwise there may be a conflict between camera and CPU pins.

Default state of CSI1/DISP1 signal after reset:
***0 - Ouptut Low**
***1 - Output High**

DESIGN NOTE:
Contacts are located on the top side of the pins of FFC connector.

CSI Camera / LVDS Connector

(Raspberry Pi compatible)



DESIGN NOTE:
Before you plug in cable into connector J12, be sure, that the correct interface is selected with the optional series resistors.

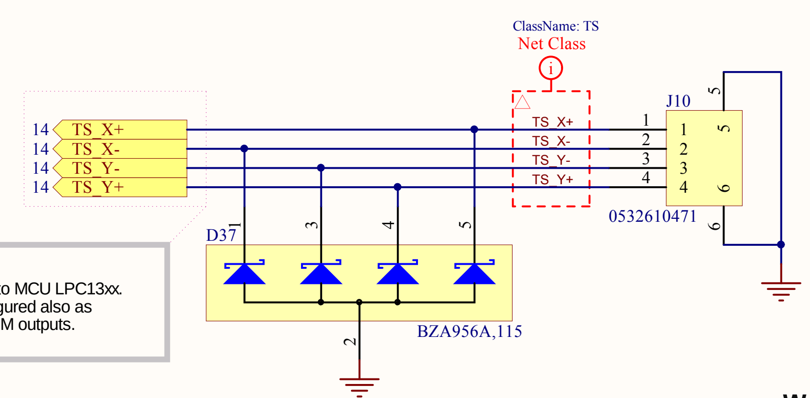
DESIGN NOTE:
CSI connector is pin compatable with Raspbery Pi camera connector.

DESIGN NOTE:
FRC - number of colors used:
High: 16,777,216 colors
Low or Open: 262,144 colors

DESIGN NOTE:
DPS - scan direction:
High: Reverse scan
Low or Open: Normal scan

DESIGN NOTE:
If FRC & DPS are used (for some LVDS displays), do not fit R154 & R156 and choose the proper combination of resistors R52, R53, R54 & R191.

Touchscreen Connector



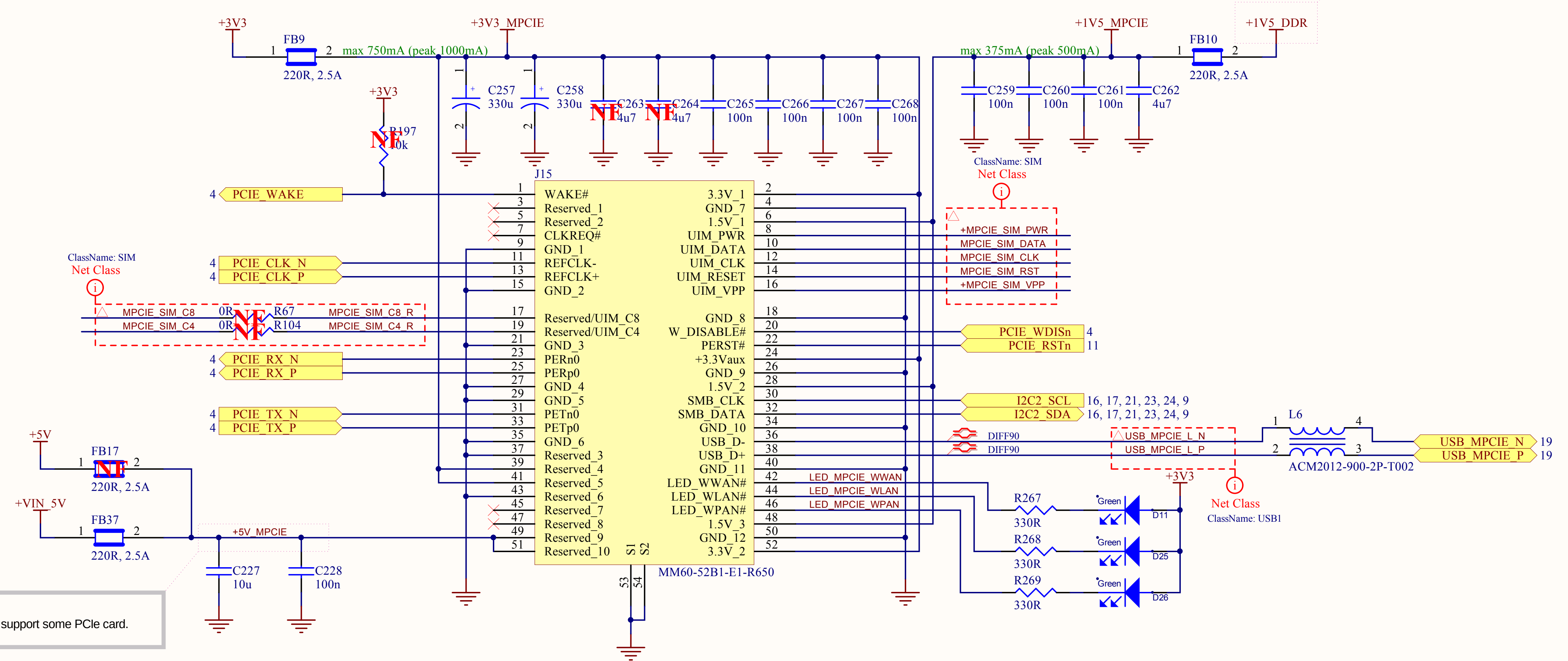
DESIGN NOTE:
Touchscreen is connected to MCU LPC13xx. These signals can be configured also as Analog inputs, GPIO or PWM outputs.

Title: OpenRex		Variant: [No Variations]	
Page Contents: [17] - LVDS, CSI, LCD, TSC.SchDoc		Checked by	
Size:	DWG NO	Revision: V1I1	
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 17 of 31	

PCIE MINI

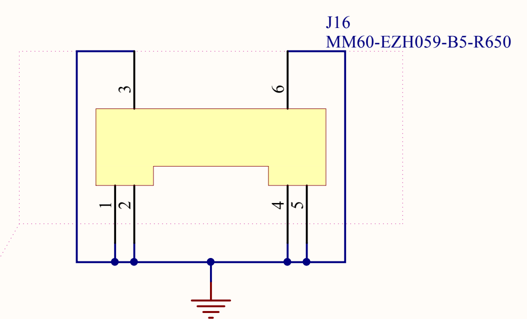
PCIe Mini Slot

LAYOUT NOTE:
To lower the influence between +1V5_PCIE and +1V5_DDR, separate +1V5 PCIe power plane from +1V5_DDR power plane close to the regulator output.



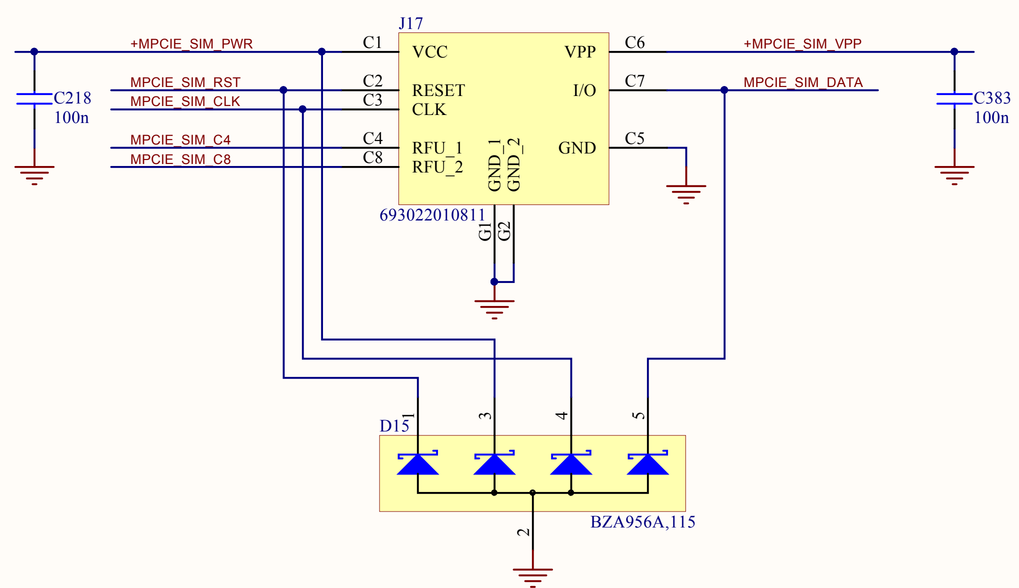
DESIGN NOTE:
+5V power is needed to support some PCIe card.

Card Latch for PCIe Mini Card



LAYOUT NOTE:
Distance between PCIe Mini connector and latch (hole to hole - the bigger ones):
X = 50.3mm
Y = 0.4mm
See also
https://jae-connectors.com/en/pdf_download_exec.cfm?param=SJ105219.pdf

SIM card for PCIe Mini



3D Model of PCIe Mini Card

CR1

Mini PCIe Card

Mini PCIe Card

LAYOUT NOTE:
This is a stand off slot. The maximum allowed component height in the PCIe Mini Card area is 2.2mm.

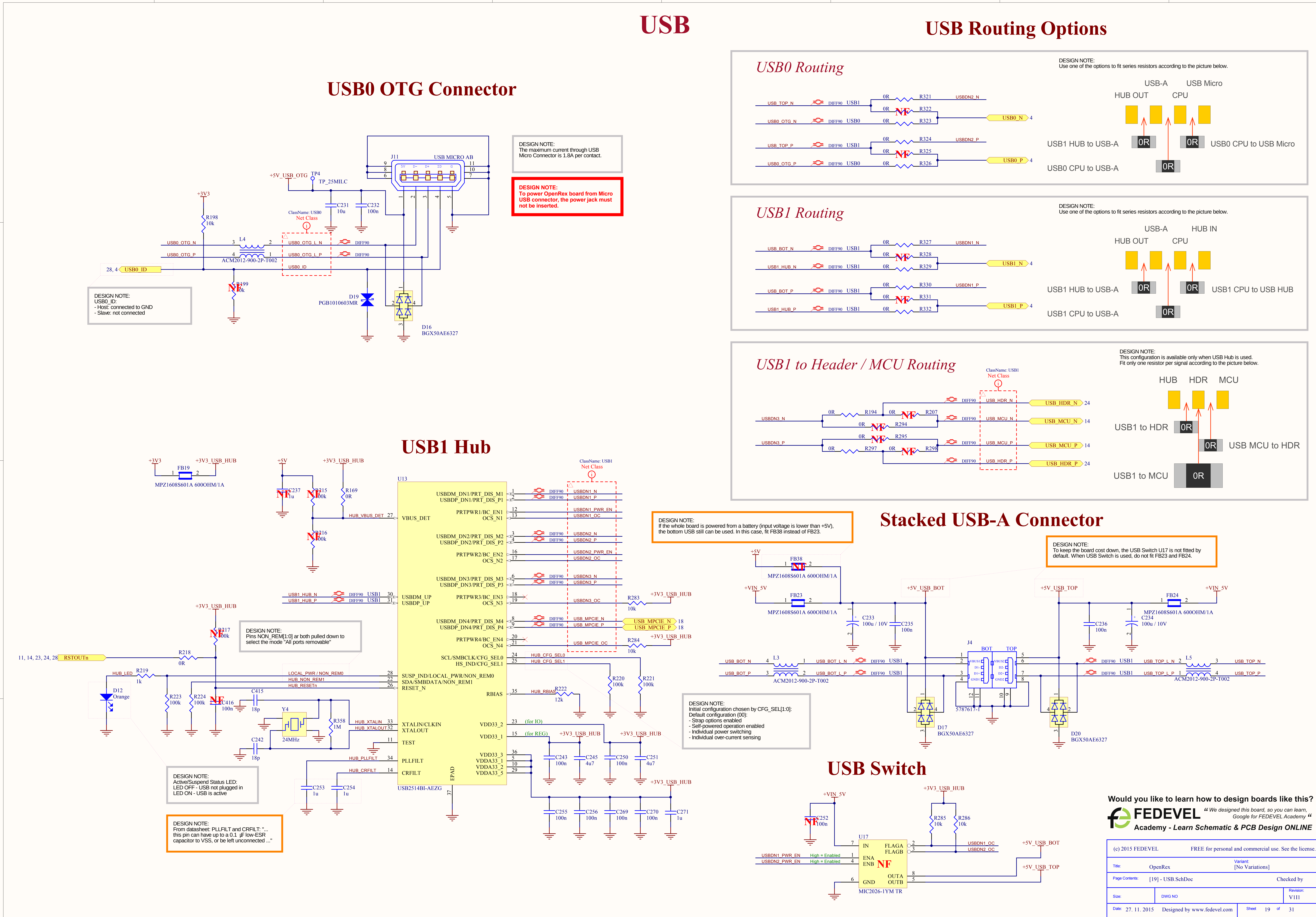
3D Model of Micro SIM Card

CR3

Micro SIM Card

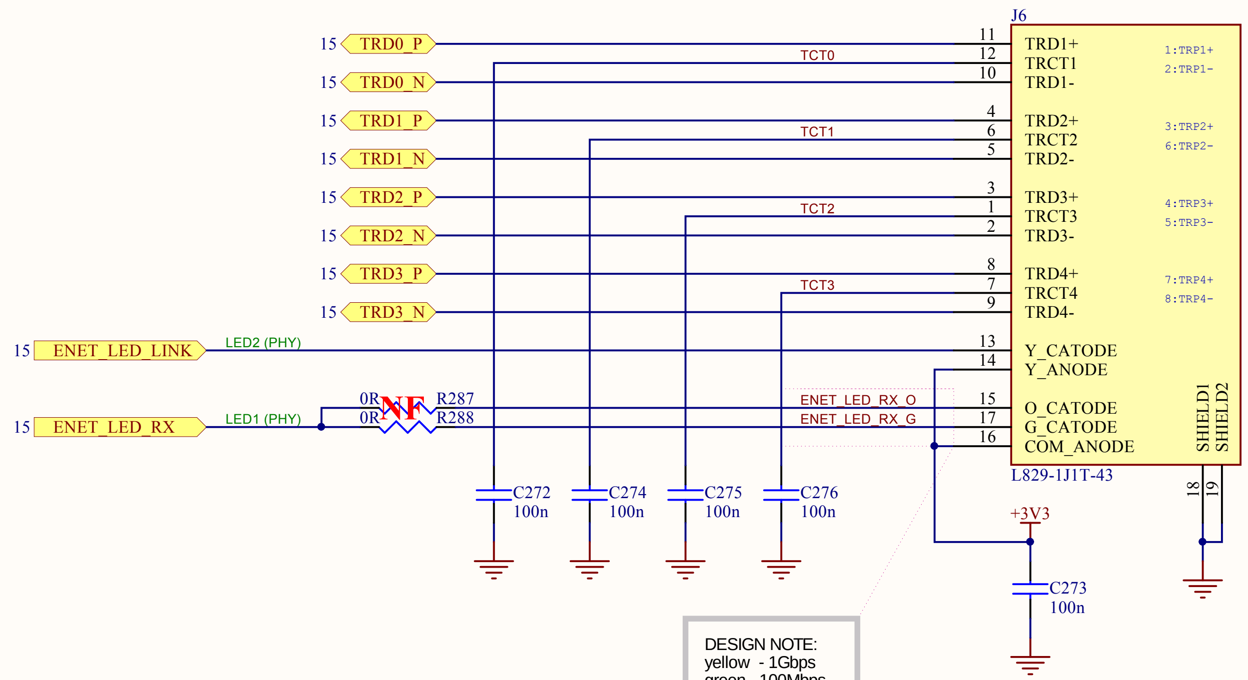
Micro SIM Card

Title: OpenRex		Variant: [No Variations]	
Page Contents: [18] - PCIE MINI.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 18 of 31	


USB
USB Routing Options
USB0 OTG Connector
USB0 Routing
USB1 Routing
USB1 to Header / MCU Routing
USB1 Hub
Stacked USB-A Connector
USB Switch
DESIGN NOTE:
The maximum current through USB Micro Connector is 1.8A per contact.
DESIGN NOTE:
To power OpenRex board from Micro USB connector, the power jack must not be inserted.
DESIGN NOTE:
USB0_ID:
- Host: connected to GND
- Slave: not connected
DESIGN NOTE:
Use one of the options to fit series resistors according to the picture below.
USB1 HUB to USB-A
USB0 CPU to USB Micro
USB0 CPU to USB-A
USB1 CPU to USB HUB
USB1 CPU to USB-A
DESIGN NOTE:
This configuration is available only when USB Hub is used.
Fit only one resistor per signal according to the picture below.
USB1 to HDR
USB MCU to HDR
USB1 to MCU
DESIGN NOTE:
If the whole board is powered from a battery (input voltage is lower than +5V), the bottom USB still can be used. In this case, fit FB38 instead of FB23.
DESIGN NOTE:
To keep the board cost down, the USB Switch U17 is not fitted by default. When USB Switch is used, do not fit FB23 and FB24.
DESIGN NOTE:
Pins NON_REM[1:0] ar both pulled down to select the mode "All ports removable"
DESIGN NOTE:
Initial configuration chosen by CFG_SEL[1:0]:
Default configuration (00):
- Strap options enabled
- Self-powered operation enabled
- Individual power switching
- Individual over-current sensing
DESIGN NOTE:
Active/Suspend Status LED:
LED OFF - USB not plugged in
LED ON - USB is active
DESIGN NOTE:
From datasheet: PLLFILT and CRFILT: "... this pin can have up to a 0.1 µF low-ESR capacitor to VSS, or be left unconnected ..."
Would you like to learn how to design boards like this?
FEDEVEL Academy - Learn Schematic & PCB Design ONLINE
"We designed this board, so you can learn, Google for FEDEVEL Academy"
(c) 2015 FEDEVEL
FREE for personal and commercial use. See the license.
Title: OpenRex
Variant: [No Variations]
Page Contents: [19] - USB.SchDoc
Checked by
Size:
DWG NO
Revision: V1I1
Date: 27. 11. 2015
Designed by www.fedevel.com
Sheet 19 of 31

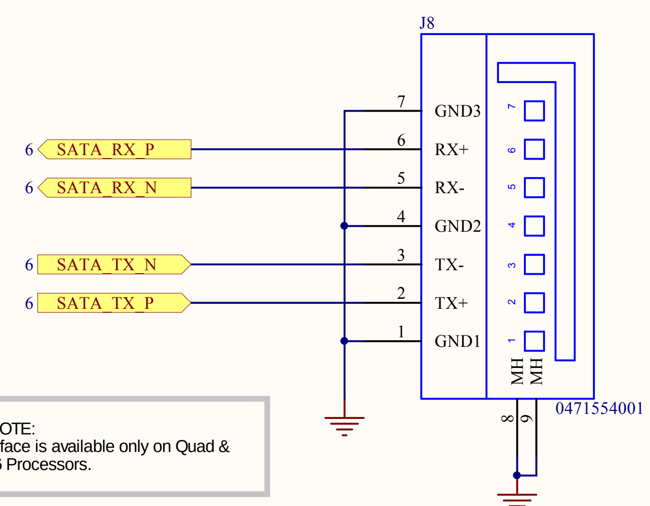
ETHERNET, SATA

RJ45 + Magnetics



DESIGN NOTE:
yellow - 1Gbps
green - 100Mbps
both - 10Mbps
Blinking - Activity

SATA



DESIGN NOTE:
SATA Interface is available only on Quad & Dual i.MX6 Processors.

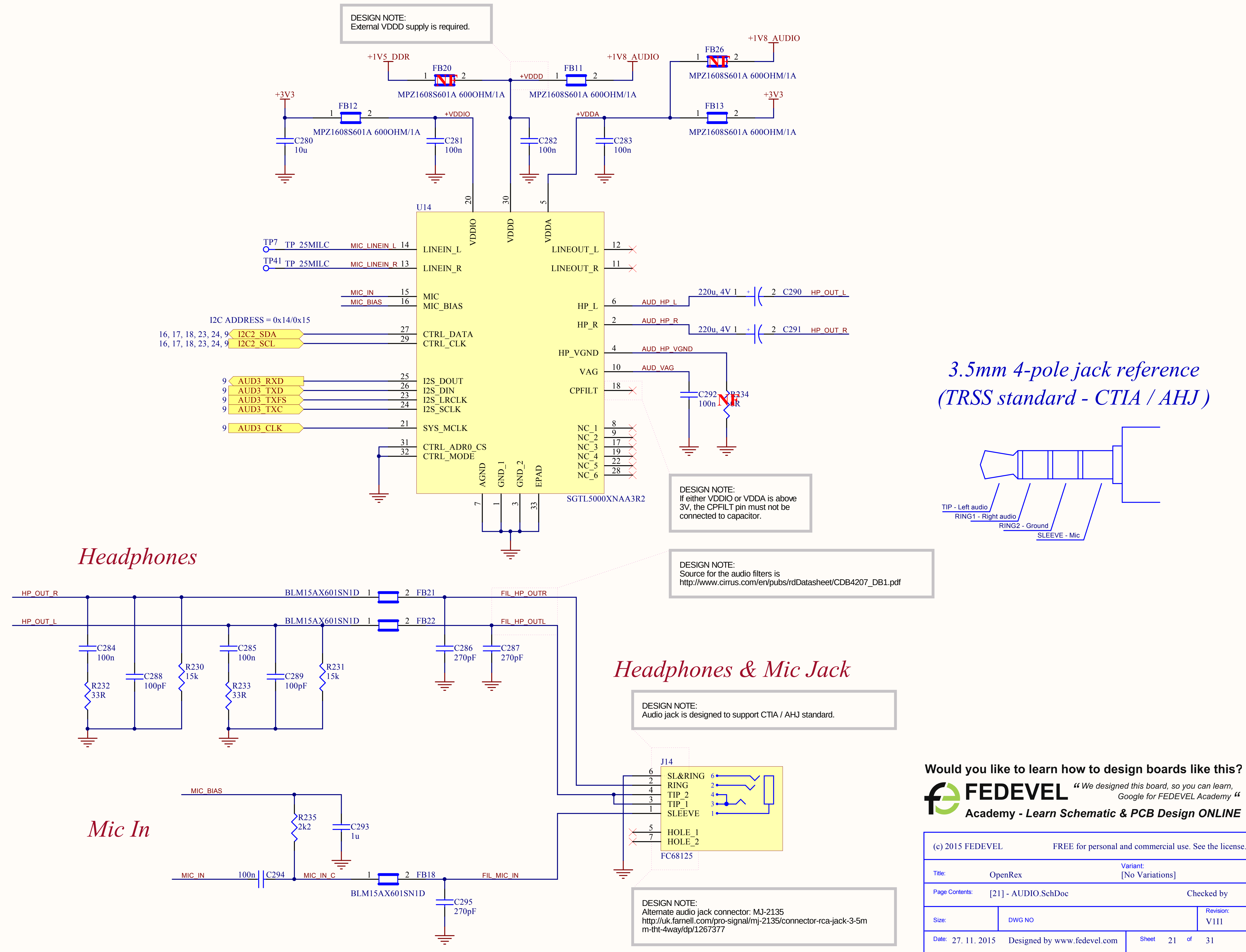
Would you like to learn how to design boards like this?

FEDEVEL “We designed this board, so you can learn, Google for FEDEVEL Academy“

Academy - *Learn Schematic & PCB Design ONLINE*

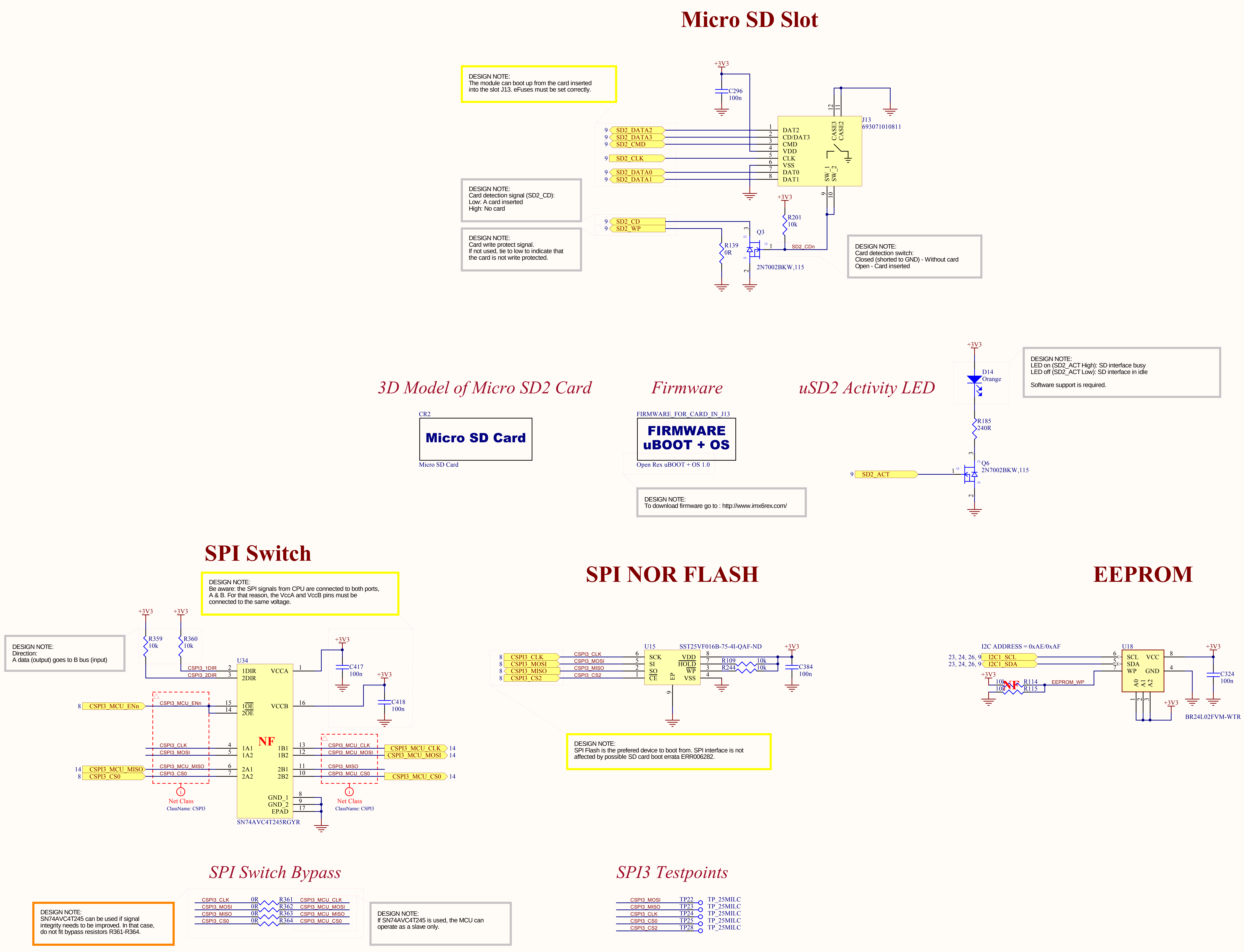
Title: OpenRex		Variant: [No Variations]	
Page Contents: [20] - ETHERNET, SATA.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 20 of 31	

AUDIO



(c) 2015 FEDEVEL	FREE for personal and commercial use. See the license.		
Title: OpenRex		Variant: [No Variations]	
Page Contents: [21] - AUDIO.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 21 of 31	

SD CARD, FLASH, EEPROM



Would you like to learn how to design boards like this?

FEDEVEL “We designed this board, so you can learn, Google for FEDEVEL Academy”

Academy - Learn Schematic & PCB Design ONLINE

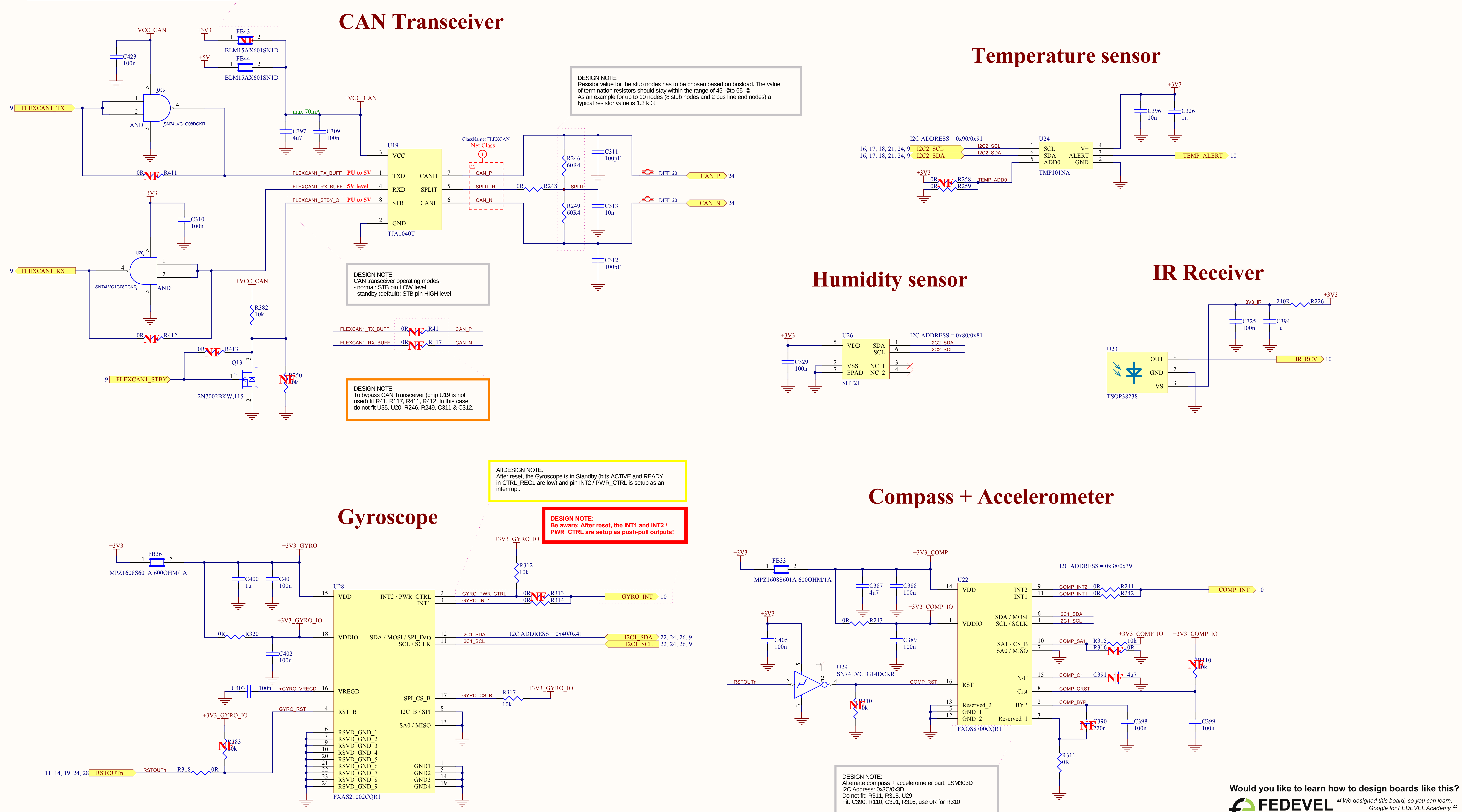
Title: OpenRex Variant: [No Variations]

Page Contents: [22] - SD CARD, SPI, FLASH, EEPROM, SchDoc Checked by

Size: DWG NO Revision: V1I1

Date: 27. 11. 2015 Designed by www.fedevel.com Sheet 22 of 31

SENSORS, IR, CAN



DESIGN NOTE:
An alternate +3V3 level CAN transceiver SN65HVD230DR can be used.
In that case, the buffers are not needed. Fit R411, R412, R413 instead.
Do not forget to change the supply voltage (fit FB43 and do not fit FB44).

DESIGN NOTE:
Resistor value for the stub nodes has to be chosen based on busload. The value of termination resistors should stay within the range of 45 Ω to 65 Ω.
As an example for up to 10 nodes (8 stub nodes and 2 bus line end nodes) a typical resistor value is 1.3 kΩ.

DESIGN NOTE:
CAN transceiver operating modes:
- normal: STB pin LOW level
- standby (default): STB pin HIGH level

DESIGN NOTE:
To bypass CAN Transceiver (chip U19 is not used) fit R41, R117, R411, R412. In this case do not fit U35, U20, R246, R249, C311 & C312.

AltDESIGN NOTE:
After reset, the Gyroscope is in Standby (bits ACTIVE and READY in CTRL_REG1 are low) and pin INT2 / PWR_CTRL is setup as an interrupt.

DESIGN NOTE:
Be aware: After reset, the INT1 and INT2 / PWR_CTRL are setup as push-pull outputs!

DESIGN NOTE:
Alternate compass + accelerometer part: LSM303D
I2C Address: 0x3C/0x3D
Do not fit: R311, R315, U29
Fit: C390, R110, C391, R316, use 0R for R310

Would you like to learn how to design boards like this?
FEDEVEL " We designed this board, so you can learn, Google for FEDEVEL Academy "
Academy - Learn Schematic & PCB Design ONLINE

Title:	OpenRex
Variant:	[No Variations]
Page Contents:	[23] - SENSORS, CAN, IR.SchDoc
Checked by	
Size:	
DWG NO	
Revision:	V1I1
Date:	27. 11. 2015
Designed by	www.fedevel.com
Sheet	23 of 31

HEADERS, UART

DESIGN NOTE:
Fit FB35 (and do not fit FB34) when battery is supplying the board. Check the maximum current for +5V first.

DESIGN NOTE:
A 2.5" SATA hard drive can be powered up through the pin J1-1 (requires +5V voltage and appr. 550mA current). In that case, be sure FB34 is fitted.

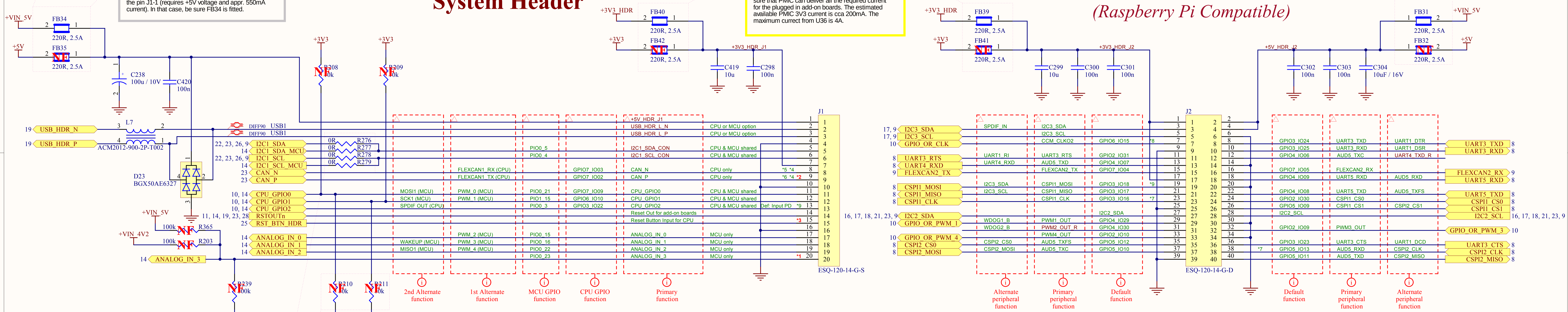
System Header

DESIGN NOTE:
To save some board cost, the strong 3V3 U36 power supply can be left unfitted. In that case, be sure that PMIC can deliver all the required current for the plugged in add-on boards. The estimated available PMIC 3V3 current is cca 200mA. The maximum currect from U36 is 4A.

Peripheral Header

(Raspberry Pi Compatible)

DESIGN NOTE:
Fit FB32 (and do not fit FB31) when battery is supplying the board. Check the maximum current for +5V first.



DESIGN NOTE:
I2C1 bus bypass options:
R276 - R279 fitted, R277 & R279 fitted (default) - system I2C connected to the J1 header and MCU
R276 & R278 fitted; R277 & R279 not fitted - system I2C connected to the J1 header, MCU is disconnected from I2C
R276 & R278 not fitted; R277 & R279 fitted - system I2C disconnected; MCU I2C or GPIO function on the J1 header. if MCU I2C is used, fit also R290 & R291 pullups.

DESIGN NOTE:
Incorrect implementation of resistors R208 - R211 can setup undefined value on CPU_CPIO0 & 1. Be sure, you disable internal pullups for MCU first. Also, be aware, that the CPU_GPIO2 pin has an internal pull down resistor enabled by default.

DESIGN NOTE:
All signals on connectors J1 & J2 are pulled high by default (unless noted otherwise). Default states may be different comparing to the Raspberry Pi pull up/down default configuration.

DESIGN NOTE:
All signals on J1 and J2 connector are 3V3 level compatible (unless otherwise noted). Connecting higher voltage may damage the board.

Exceptions:
***1 This pin my be connected to input voltage (when R239, R203 or R365 is fitted) to support input voltage monitoring**
***2 Ouput of this signal can be as high as +5V**
***3 Be careful: This pin may be connected to +3V0_SVNVS**

DESIGN NOTE:
*4 Pins CANH & CANL can be used as standard GPIOs or FLEXCAN pins. Before using these functions, be sure that the CAN Transceiver is not fitted (U19, U2o, U35, R246, R249, C311 & C312 NF) and signals are bypassed (R41, R117, R411, R412 fitted).

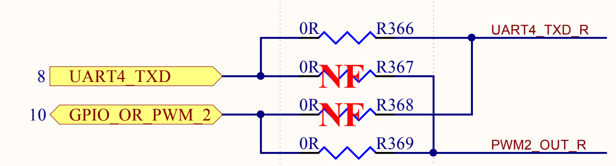
DESIGN NOTE:
*5 When CANL signal is bypassed and buffer U20 is fitted, this pin can be used as a 5V tolerant input.

*6 When CANH signal is bypassed and buffer U35 is fitted, this pin can be used as a 5V CPU output.

DESIGN NOTE:
*7 These signals have series 22R resistor in signal path.

*8 If I2S Audio (AUD5) is used throught the J2 header, GPIO_OR_CLK can be used as the master clock.

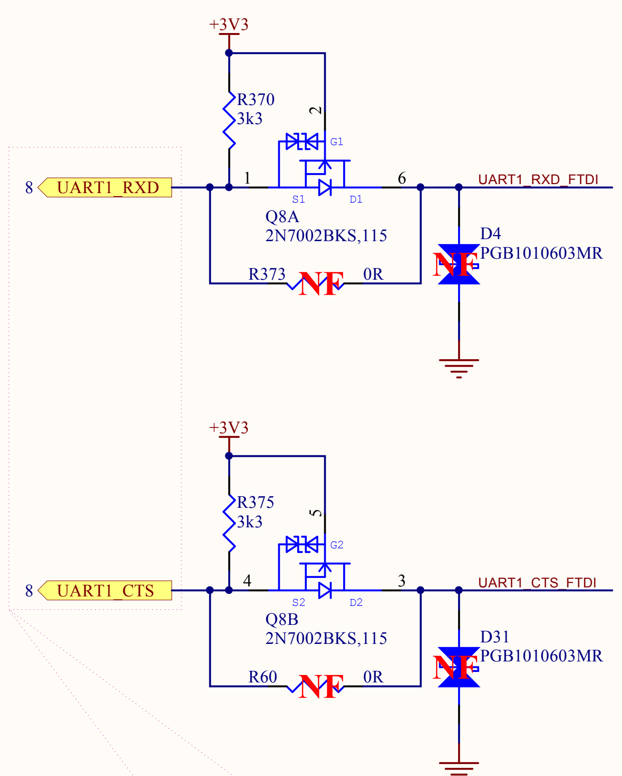
DESIGN NOTE:
*9 These signals can be used as an optional SPDIF digital audio interface:
- SPDIF_OUT: use CPU_GPIO2
- SPDIF_IN: use I2C3_SDA. In this case, do not place any other devices on the I2C3 bus.



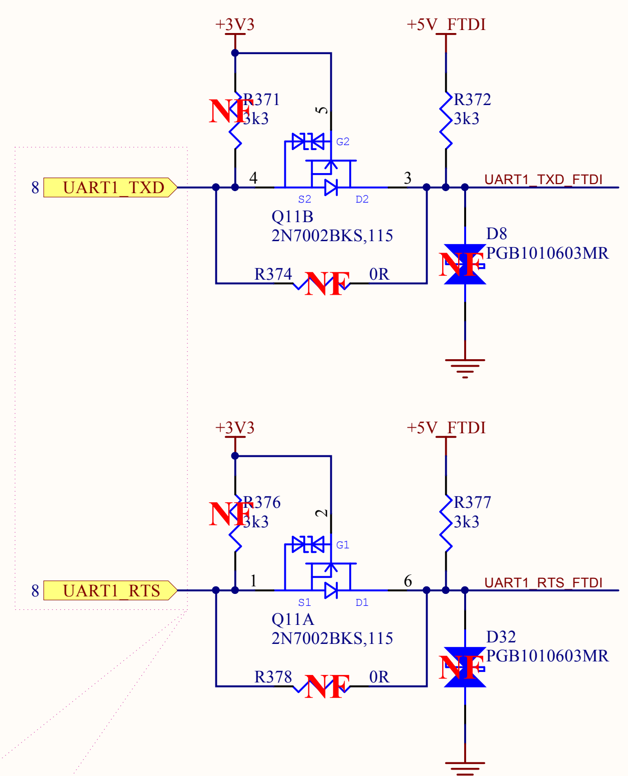
DESIGN NOTE:
If some add-on boards (compatible with short Raspberry Pi connector) require PWM Signal connected to J2-pin12, these signals can be swapped using resistors R366-R369.

UART 1 - Debug console (+3V3)

Buffers for CPU Input Pins



Buffers for CPU Output Pins



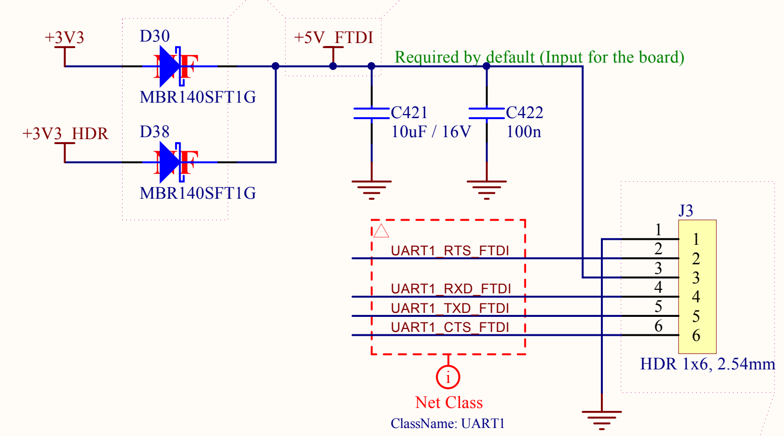
DESIGN NOTE:
Buffers for UART1 are designed to isolate the CPU when the board is turned off and FTDI cable is still connected. Without the isolation, leaking current from the plugged FTDI cable can prevent CPU from booting.

DESIGN NOTE:
If isolation is not required, buffers can by bypassed through R60, R373, R374 and R378 resistors.

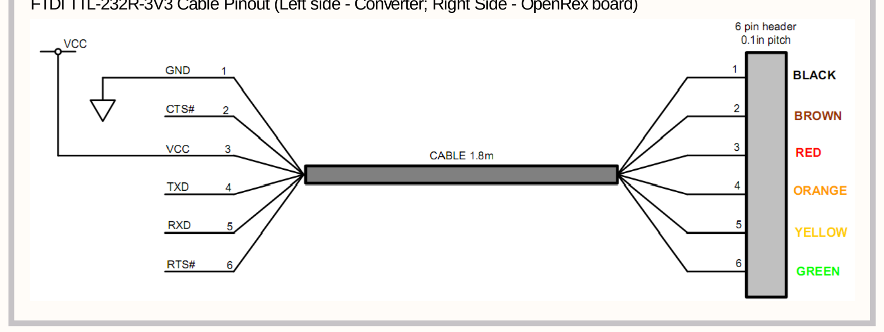
Serial console header

DESIGN NOTE:
In the case, when J3 is not used for debugging, but as a standard UART interface,+3V3 power can be provided on J3 pin 3 through D30 or D38.

DESIGN NOTE:
If isolation circuits are fitted, the UART signals on J3 support signal levelling defined by device connected to the J3 and voltage connected to J3 pin 3 (e.g. 3V3, 5V, ...)



DESIGN NOTE:
FTDI TTL-232R-3V3 Cable Pinout (Left side - Converter; Right Side - OpenRex board)



DESIGN NOTE:
Serial console header is designed to be used with FTDI TTL-232R-3V3 TTL to USB Serial Converter Cable by default:
http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

Title: OpenRex		Variant: [No Variations]	
Page Contents: [24] - HEADERS, UART.SchDoc			Checked by
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 24 of 31	

LEDS, BUTTONS

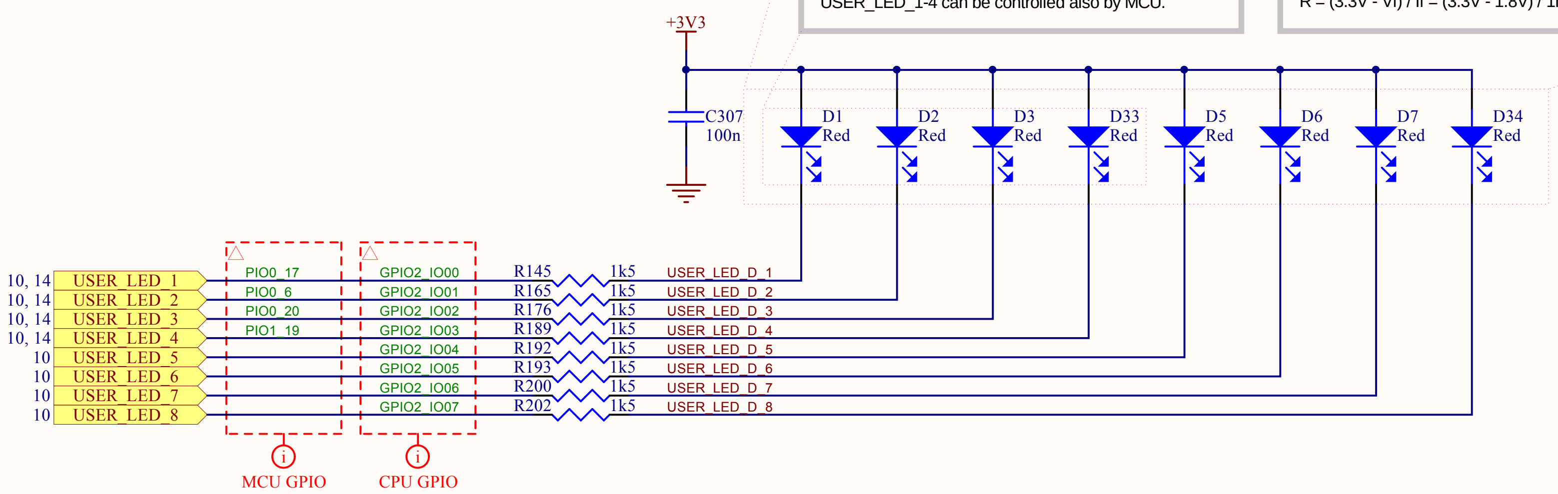
User LEDS

DESIGN NOTE:
When driving LEDs, do not set the pins as outputs. Set them as an open drain and use internal pullup to prevent conflict with MCU pins. Do the same for MCU.

DESIGN NOTE:
i.MX6 datasheet does not show the maximum CPU output pin current. Only what is guaranteed, is a 1mA testing current mentioned in Table 22 (datasheet IMX6DQCEC.pdf).

DESIGN NOTE:
USER_LED_1-4 can be controlled also by MCU.

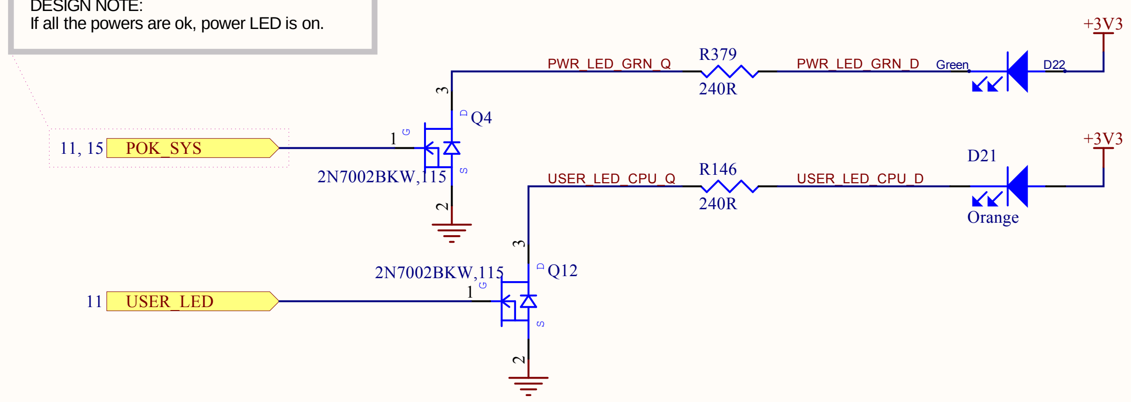
DESIGN NOTE:
Series resistor calculation (for forward current 1mA)
R = (3.3V - Vf) / If = (3.3V - 1.8V) / 1mA = 1.5k Ohm



LEDs

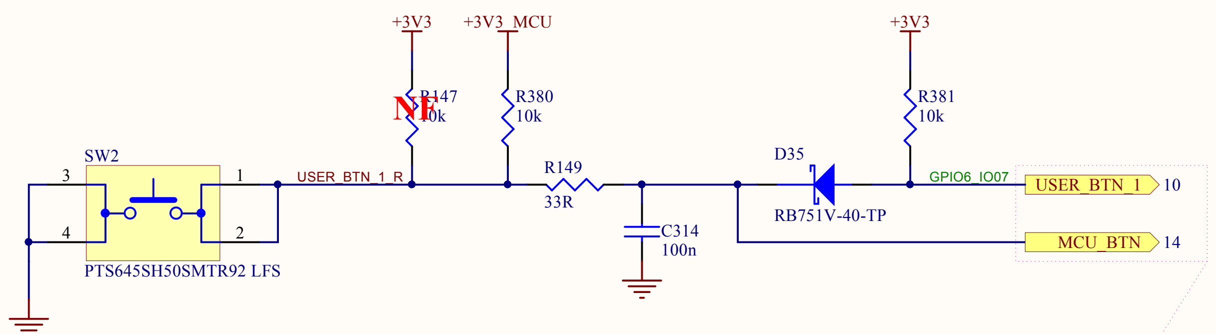
Power, CPU User LEDs

DESIGN NOTE:
If all the powers are ok, power LED is on.



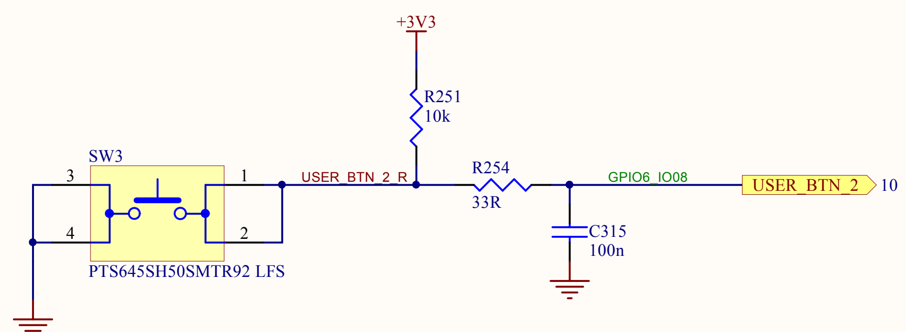
User / Android Buttons

Home / Wake Up Button

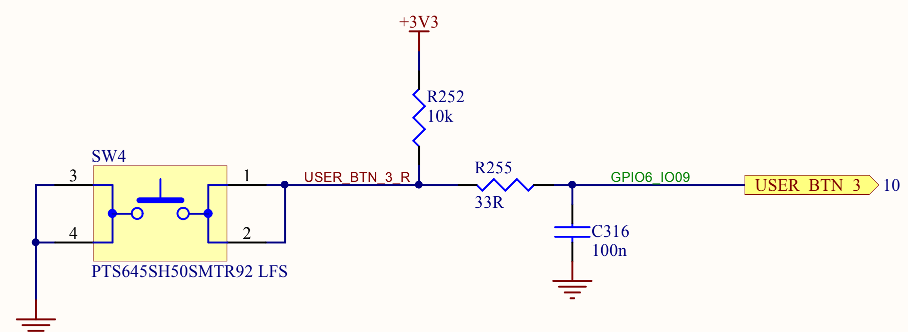


DESIGN NOTE:
Home / Wake up button can be used by both: CPU and MCU.

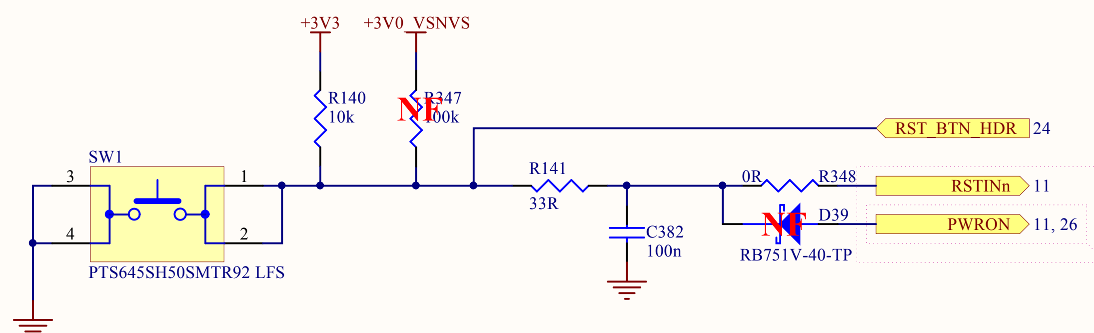
Back / Volume- Button



Recent / Volume+ Button



Reset / Power Button

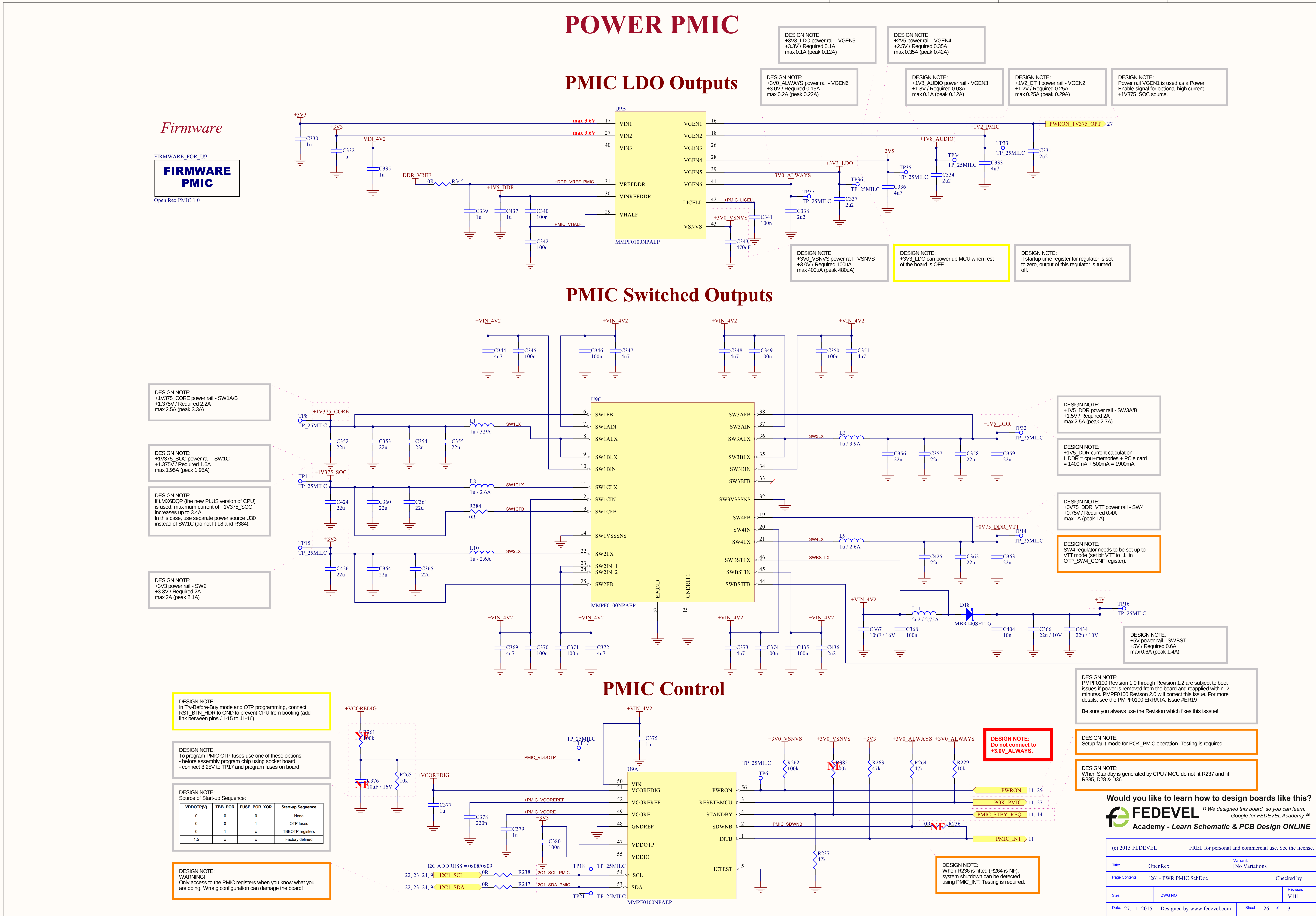


DESIGN NOTE:
Reset / Power On-Off Button function:
- RSTINn - the button resets the CPU and peripherals (default) - Fit R140 & R348, do not fit R347 & D39
- PWRON - the button is connected to PMIC and resets or turns on / off the whole board - Fit R347 & D39, do not fit R140 & R348

DESIGN NOTE:
PMIC PWRON button function (based on PWRON_CFG setting in PMIC registers)
- PWRON_CFG = Low (level sensitive): reset all the sources when button pressed
- PWRON_CFG = High (edge sensitive): button acts as a power signal for the board
  - button pressed momentarily - board turns on
  - button pressed for more than 4 seconds - boards turns off or put to sleep mode

Title: OpenRex		Variant: [No Variations]	
Page Contents: [25] - LEDS, BUTTONS.SchDoc		Checked by	
Size:	DWG NO		Revision: V111
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 25 of 31	

POWER PMIC



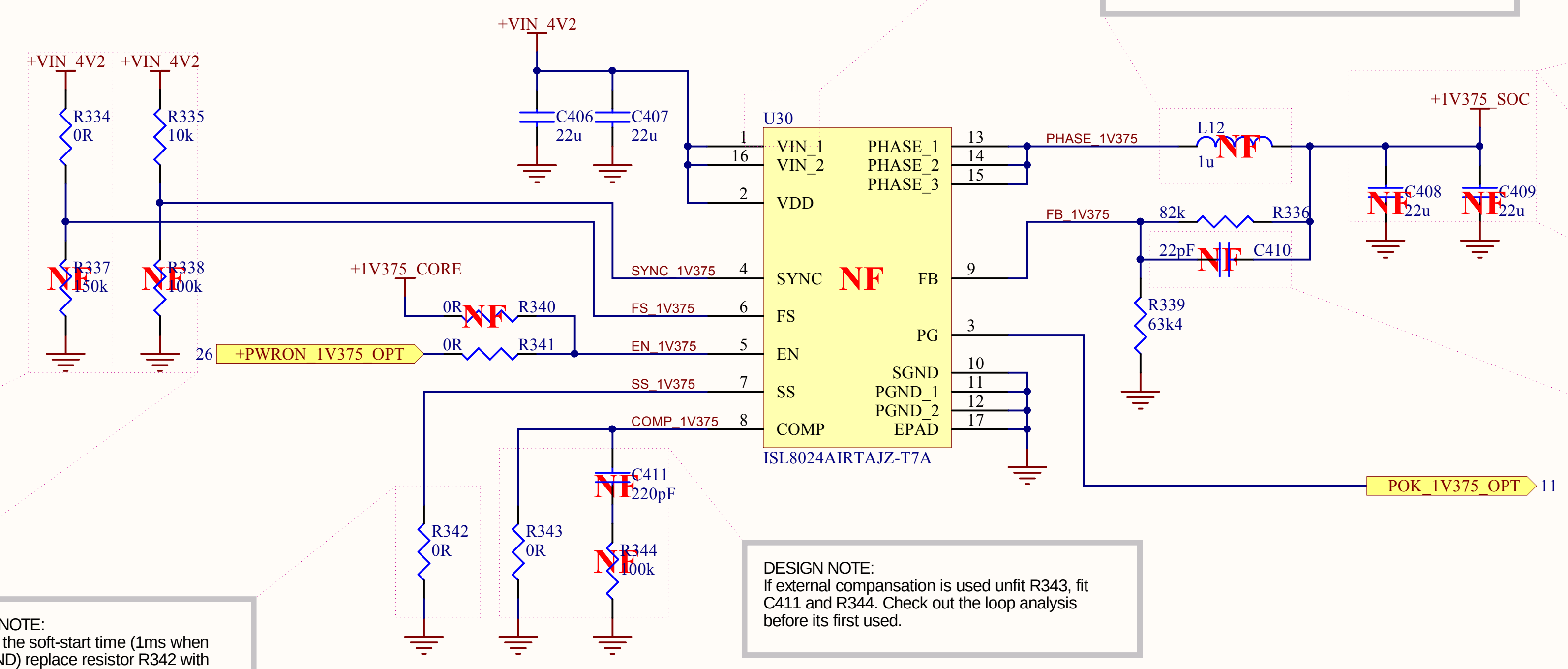
VDDOTP(V)	TBB_POR	FUSE_POR_XOR	Start-up Sequence
0	0	0	None
0	0	1	OTP fuses
0	1	x	TBBOTP registers
1.5	x	x	Factory defined

PWR +1V375_SOC OPT, +3V3 OPT

Optional +1V375_SOC

DESIGN NOTE:
Fit this optional +1V375_SOC regulator to support iMX6DQP (the new iMX6 PLUS CPU), which requires higher current.

DESIGN NOTE:
In case this Optional +1V375_SOC is used fit U30, L12, C408 and C409.
Be sure R351 is fitted, L8 and R384 not fitted.



DESIGN NOTE:
+1V375_SOC / max 4A / peak 5.2A
(Required 3.4A)

DESIGN NOTE:
Rest of the output capacitors are placed on PMIC page.

DESIGN NOTE:
resistor values for output voltage 1V375:
R336=R339*(Vout/Vref-1)=63.4k*(1.375/0.6-1)=81.892k
backward control:
Vout=Vref*(R336+R339)/R339=0.6*(82k+63.4k)/63.4k=1.376V

DESIGN NOTE:
If feedback loop needs to be compansated fit C410. Check out the loop analysis before its first used.

DESIGN NOTE:
Default switching frequency 1MHz (FS tied to Vin). Use R337 to adjust the operating frequency.

DESIGN NOTE:
Mode selection (SYNC):
Vin - PWM mode
GND - PFM mode

DESIGN NOTE:
To adjust the soft-start time (1ms when tied to GND) replace resistor R342 with a capacitor smaller than 33nF.

DESIGN NOTE:
If external compansation is used unfit R343, fit C411 and R344. Check out the loop analysis before its first used.

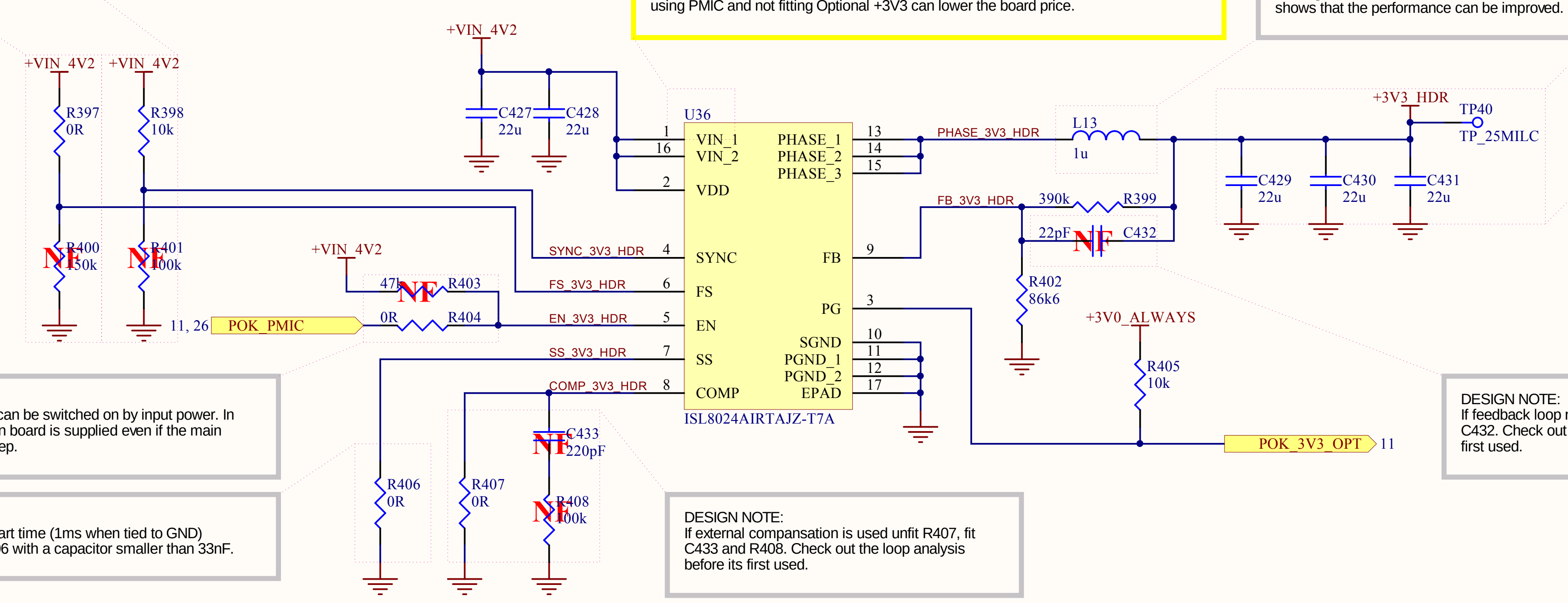
Optional +3V3

DESIGN NOTE:
Mode selection (SYNC):
Vin - PWM mode
GND - PFM mode

DESIGN NOTE:
Default switching frequency 1MHz (FS tied to Vin). Use R400 to adjust the operating frequency.

DESIGN NOTE:
This Optional +3V3 regulator can deliver up to 4A to the board to board headers and can be used to supply number of add-on boards.
In comparision, the PMIC can deliver only around 200mA to the headers, however using PMIC and not fitting Optional +3V3 can lower the board price.

DESIGN NOTE:
The higher inductor value can be selected if the testing shows that the performance can be improved.



DESIGN NOTE:
+3V3_HDR / max 4A / peak 5.2A
(Required 3A)

DESIGN NOTE:
resistor values for output voltage 3V3:
R339=R402*(Vout/Vref-1)=86.6k*(3.3/0.6-1)=389.7k
backward control:
Vout=Vref*(R339+R402)/R402=0.6*(86.6k+390k)/86.6k=3.302V

DESIGN NOTE:
+3V3_HDR source can be switched on by input power. In this case, the add-on board is supplied even if the main board is off or in sleep.

DESIGN NOTE:
To adjust the soft-start time (1ms when tied to GND) replace resistor R406 with a capacitor smaller than 33nF.

DESIGN NOTE:
If external compansation is used unfit R407, fit C433 and R408. Check out the loop analysis before its first used.

DESIGN NOTE:
If feedback loop needs to be compansated fit C432. Check out the loop analysis before its first used.

(c) 2015 FEDEVEL	FREE for personal and commercial use. See the license.
Title: OpenRex	Variant: [No Variations]
Page Contents: [27] - PWR 1V375 OPT, 3V3 OPT.SchDoc	Checked by
Size: DWG NO	Revision: V1I1
Date: 27. 11. 2015 Designed by www.fedevel.com	Sheet 27 of 31

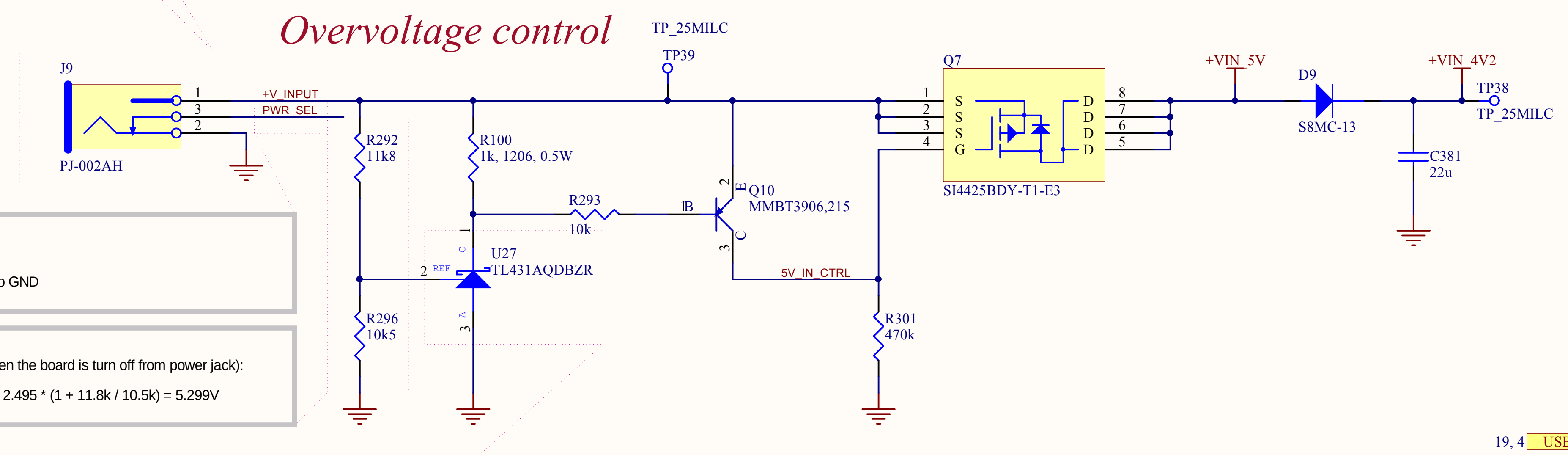
PWR IN, MECHANICAL, DOC

Power Input (+5V DC)

DESIGN NOTE:
Input voltage (+VIN_5V): +4.9 - 5.2V
Required max. current 7.5A (max. 5.5A through D9)

DESIGN NOTE:
J9 maximum current is 5A.

Overvoltage control



DESIGN NOTE:
Power jack connector insertion switch:
Jack plugged in - PWR_SEL high Z
Jack removed - PWR_SEL connected to GND

DESIGN NOTE:
Reference voltage (the input voltage when the board is turn off from power jack):
V_out_off = 5.3V; V_ref = 2.495V
V_out_off = V_ref * (1 + R292 / R296) = 2.495 * (1 + 11.8k / 10.5k) = 5.299V

DESIGN NOTE:
Chip U27 is a shunt regulator and is used to control the overvoltage protection.

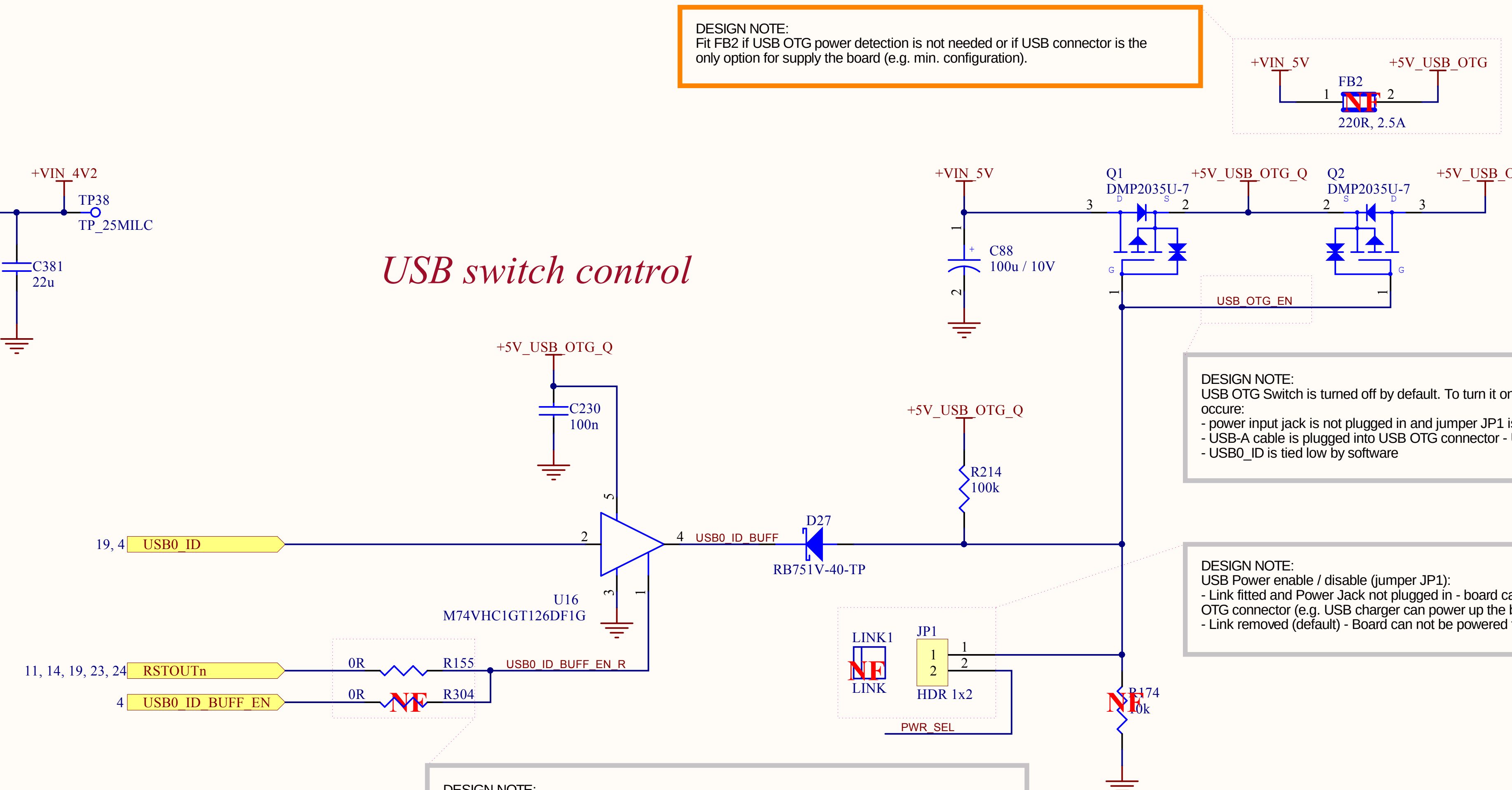
When the voltage on divider R292-R296 is below internal reference (+V_INPUT is lower then 5.3V), then input voltage is connected to the system input power (+VIN_5V).

If +V_INPUT is above +5.3V, transistor Q7 is turn off to protect the board.

USB0 OTG Power Switch

DESIGN NOTE:
Fit FB2 if USB OTG power detection is not needed or if USB connector is the only option for supply the board (e.g. min. configuration).

USB switch control



DESIGN NOTE:
USB OTG Switch is turned off by default. To turn it on, one of these coditions must occure:
- power input jack is not plugged in and jumper JP1 is shortened
- USB-A cable is plugged into USB OTG connector - USB act as a host
- USB0_ID is tied low by software

DESIGN NOTE:
USB Power enable / disable (jumper JP1):
- Link fitted and Power Jack not plugged in - board can be powered through USB OTG connector (e.g. USB charger can power up the board)
- Link removed (default) - Board can not be powered from USB OTG

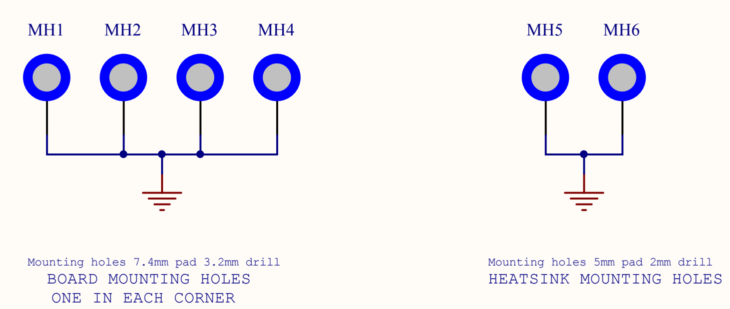
DESIGN NOTE:
Until the board is not fully configured (until BUF_SYS_RSTn is low), USB0_ID will not affect USB OTG switch (will be off). The USB power switch can also be manually controled from CPU (through USB0_ID_BUFF_EN signal).

License

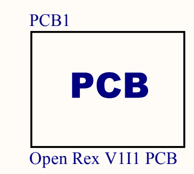
I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
I2C1	*PMIC control*	*0x08 / 0x09*
	Compass + Accelerometer	*0x38 / 0x39*
	Gyroscope	*0x40 / 0x41*
	EEPROM	*0xAE / 0xAF*
	MCU (LPC13xx)	
	For general use (on header J1)	
I2C2	*Audio*	*0x14 / 0x15*
	HDMI	*0x60 , 0xA1*
	Humidity sensor	*0x80 / 0x81*
	Temperature sensor	*0x90 / 0x91*
	Mini PCIe Card	
	CSI / LVDS Connector	
	For general use (on header J2)	
I2C3	*DISP0 / CSI1 Connector*	
	For general use (on header J2)	

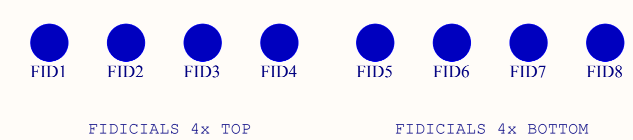
Mounting Holes



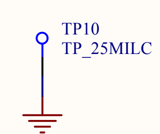
PCB



Fiducials



Gnd Testpoint



Would you like to learn how to design boards like this?

FEDEVEL Academy - Learn Schematic & PCB Design ONLINE

“We designed this board, so you can learn, Google for FEDEVEL Academy”

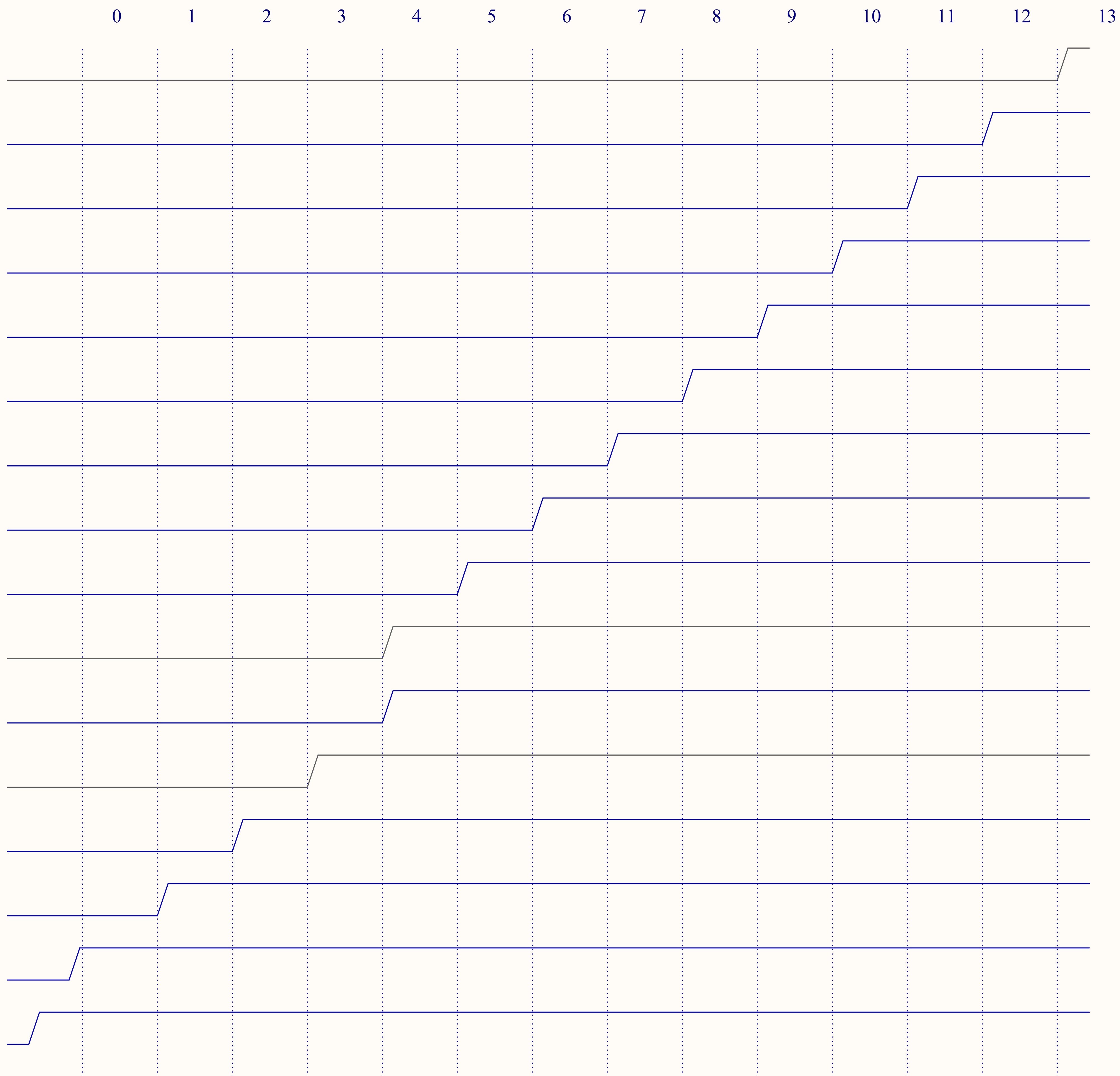
(c) 2015 FEDEVEL	FREE for personal and commercial use. See the license.		
Title: OpenRex		Variant: [No Variations]	
Page Contents: [28] - PWR IN, MECH, DOC.SchDoc		Checked by	
Size:	DWG NO		Revision: V1I1
Date: 27. 11. 2015	Designed by www.fedevel.com	Sheet 28 of 31	

POWER SEQUENCING

FROM	OTHER POWERS	LEVEL	USED BY
VGEN5	+3V3_LDO	3.3V	MCU (optional)
PMIC	+DDR_VREF	0.75V	ref. for DDR memories (from +1V5_DDR)
CPU	+1V2_VDD_ARM_CAP	0.950 - 1.25V	core caps, CPU
CPU	+1V1_VDDSOC_CAP	1.175 - 1.25V	core caps, CPU-sata, CPU-pcie, CPU-hdmi
CPU	+VDDPU	1.175 - 1.25V	core caps

POWER UP SEQUENCE

PMIC NAME / CHIP	NAME	LEVEL	USED BY
U32 (page 15)	+1V2_REG	1.2V	ethernet phy (optional)
U36 (page 27)	+3V3_HDR	3.3V	headers
VGEN3	+1V8_AUDIO	1.8V	audio codec
VGEN2	+1V2_PMIC	1.2V	ethernet phy
SWBST	+5V	5V	CPU, chips, headers
VGEN4	+2V5	2.5V	CPU, ethernet phy
SW2	+3V3	3.3V	CPU, chips, peripherals
SW4	+0V75_DDR_VTT	0.75V	memories termination
SW3AB	+1V5_DDR	1.5V	CPU, memories
U30 (page 27)	+1V375_SOC	1.375V	CPU core voltage (optional from U30)
SW1C	+1V375_SOC	1.375V	CPU core voltage (default from PMIC)
VGEN1	+PWRON_OPT_1V375	1.2V	Enable signal for +1V375_SOC chip U30 (opt., not used as a power)
SW1AB	+1V375_CORE	1.375V	CPU core voltage
VGEN6	+3V0_ALWAYS	3.0V	CPU, reset buffer, CPU config
VSNVS	+3V0_VSNVS	3.0V	PMIC PWRON
	+VIN	4.8V-5.3V	PMIC, USB connectors, headers



TIME

Would you like to learn how to design boards like this?
FEDEVEL "We designed this board, so you can learn, Google for FEDEVEL Academy"
Academy - Learn Schematic & PCB Design ONLINE

Title: OpenRex Variant: [No Variations]
Page Contents: [29] - POWER SEQUENCING.SchDoc Checked by
Size: DWG NO Revision: V1I1
Date: 27. 11. 2015 Designed by www.fedevel.com Sheet 29 of 31

REVISION HISTORY

Designator
[01] - COVER PAGE.SchDoc

Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - CPU - DDR3, DDR3 MEM.SchDoc

Designator
[04] - CPU - PCIE, USB.SchDoc

Designator
[05] - CPU - HDMI, LVDS.SchDoc

Designator
[06] - CPU - ETHERNET, SATA.SchDoc

Designator
[07] - CPU - CSI, DISP.SchDoc

Designator
[08] - CPU - SPI, UART.SchDoc

Designator
[09] - CPU - SD, AUDIO, I2C, CAN.SchDoc

Designator
[10] - CPU - GPIO, PWM, LEDS, BUTTONS.SchDoc

Designator
[11] - CPU - JTAG, CONTROL.SchDoc

Designator
[12] - CPU - POWER.SchDoc

Designator
[13] - CPU - UNUSED.SchDoc

Designator
[14] - MCU.SchDoc

Designator
[15] - ETHERNET PHY.SchDoc

Designator
[16] - HDMI.SchDoc

Designator
[17] - LVDS, CSI, LCD, TSC.SchDoc

Designator
[18] - PCIE MINI.SchDoc

Designator
[19] - USB.SchDoc

Designator
[20] - ETHERNET, SATA.SchDoc

Designator
[21] - AUDIO.SchDoc

Designator
[22] - SD CARD, SPI, FLASH, EEPROM,.SchDoc

Designator
[23] - SENSORS, CAN, IR.SchDoc

Designator
[24] - HEADERS, UART.SchDoc

Designator
[25] - LEDS, BUTTONS.SchDoc

Designator
[26] - PWR PMIC.SchDoc

Designator
[27] - PWR 1V375 OPT, 3V3 OPT.SchDoc

Designator
[28] - PWR IN, MECH, DOC.SchDoc

Designator
[29] - POWER SEQUENCING.SchDoc

Designator
[30] - REVISION HISTORY.SchDoc

NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

Title: OpenRex	Variant: [No Variations]
Page Contents: OpenRex_V1I1 Project.SchDoc	Checked by
Size:	DWG NO	Revision: V1I1
Date: 27. 11. 2015 Designed by www.fedevel.com	Sheet 31 of 31