

Layer	Stack up	Description	Base Thickness	Finish Thickness	Mask Thickness	εr	Impedance ID	Type	Notes-1
1		Soldermask			0.787	4.100		SolderMask	10
		Foil	0.472	1.378			1, 2, 3	Foil	0
2		VT47-1080	2.949	2.949		4.000		PREPREG	
		Foil	0.354	1.260				Foil	0
		VT47-106	2.087	2.087		4.000		PREPREG	
		VT47-106	2.087	2.087		4.000		PREPREG	
3		VT-47	0.700	1.378		4.600	4, 5, 6	Core	
4		VT-47	8.000	8.000				Core	
		VT47-2113	3.780	3.780		4.000		PREPREG	
		VT-47	0.700	0.700				Core	
		VT-47	4.000	4.000		4.120		Core	
5		VT-47	0.700	0.700				Core	
6	VT47-106	2.087	2.087		4.000		PREPREG		
	VT47-106	2.087	2.087		4.000		PREPREG		
7	VT-47	0.700	0.700				Core		
8	VT-47	4.000	4.000		4.120		Core		
	VT47-2113	3.780	3.780		4.000		PREPREG		
9	VT-47	0.700	0.700				Core		
10	VT-47	8.000	8.000		4.600	7, 8, 9	Core		
	VT47-106	0.700	1.378				Core		
	VT47-106	2.087	2.087		4.000		PREPREG		
	VT47-106	2.087	2.087		4.000		PREPREG		
11	Foil	0.354	1.260				Foil	0	
	VT47-1080	2.949	2.949		4.000		PREPREG		
12	Foil	0.472	1.378			10, 11, 12	Foil	0	
	Soldermask				0.787	4.100		SolderMask	10

Copper Thickness = 12.230 | Dielectric Thickness = 49.976 | Solder Mask Thickness = 1.575 | Stack Up Thickness = 62.206 | Stack Up Thickness with Solder Mask = 63.781 |


Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Trace Separation	Ground Strip Separation	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)
1		Coated Microstrip 1B	1	2	0	3.661	0.000	0.000	0	55.060	55.000	10.000
2		Edge Coupled Coated Microstrip 1B	1	2	0	3.976	4.488	0.000	0	90.060	90.000	10.000
3		Edge Coupled Coated Microstrip 1B	1	2	0	3.543	6.299	0.000	0	100.300	100.000	10.000
4		Offset Stripline 1B1A	3	2	4	3.150	0.000	0.000	0	53.620	55.000	10.000

StackName: iMX6_Rex_V111_PCB_12L_VT47_mv	Version: 1	Revision:	Modification:	Date of Revision:	Editor	Page 1/3	
Date: 31/10/2013	Associated Documents:						
Author: DM							
Department: IDS							
Site: Tewkesbury							


Impedance ID	Structure Image	Structure Name	Impedance Signal Layer	Ref. Plane 1 in Layer	Ref. Plane 2 in Layer	Lower Trace Width	Trace Separation	Ground Strip Separation	Broadside 2nd Layer	Calculated Impedance	Target Impedance	Tol (+/- %)
5		Edge Coupled Offset Stripline 1B1A	3	2	4	3.346	4.528	0.000	0	88.390	90.000	10.000
6		Edge Coupled Offset Stripline 1B1A	3	2	4	3.346	7.677	0.000	0	98.390	100.000	10.000
7		Offset Stripline 1B1A	10	9	11	3.150	0.000	0.000	0	53.620	55.000	10.000
8		Edge Coupled Offset Stripline 1B1A	10	9	11	3.346	4.528	0.000	0	88.390	90.000	10.000
9		Edge Coupled Offset Stripline 1B1A	10	9	11	3.346	7.677	0.000	0	98.390	100.000	10.000
10		Coated Microstrip 1B	12	11	0	3.661	0.000	0.000	0	55.060	55.000	10.000
11		Edge Coupled Coated Microstrip 1B	12	11	0	3.976	4.488	0.000	0	90.060	90.000	10.000
12		Edge Coupled Coated Microstrip 1B	12	11	0	3.543	6.299	0.000	0	100.300	100.000	10.000

Column Position	Drill Image	1st Layer	2nd Layer	Drill Type	Fill Type	Minimum Size	Data Filenames
1		1	12	Mechanical PTH	None	0.008	
2		1	2	Laser PTH	None	3.937	
3		2	3	Laser PTH	None	3.937	
2		12	11	Laser PTH	None	3.937	
3		11	10	Laser PTH	None	3.937	

StackName: iMX6_Rex_V111_PCB_12L_VT47_mv	Version: 1	Revision:	Modification:	Date of Revision:	Editor	Page 2/3	
Date: 31/10/2013	Associated Documents:						
Author: DM							
Department: IDS							
Site: Tewkesbury							

Column Position	Drill Image	1st Layer	2nd Layer	Drill Type	Fill Type	Minimum Size	Data Filenames
4		3	10	Mechanical PTH	None	7.874	

Notes

StackName: iMX6_Rex_V111_PCB_12L_VT47_mv	Version: 1	Revision:	Modification:	Date of Revision:	Editor	Page 3/3	
Date: 31/10/2013	Associated Documents:						
Author: DM							
Department: IDS							
Site: Tewkesbury							