OpenRex

Variant: Production

10. 1. 2016
V1I1

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

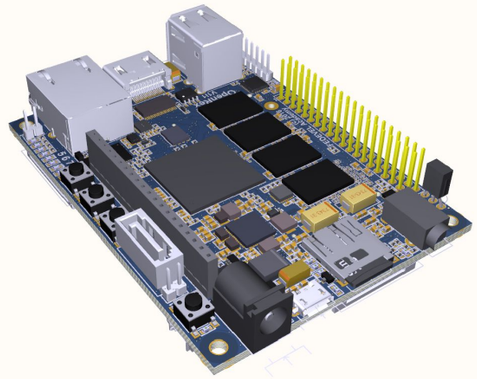
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

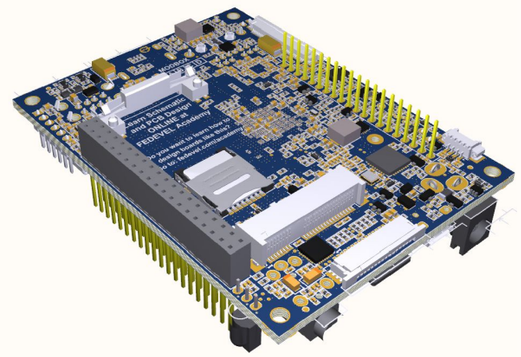
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW



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OpenRex
(Block Diagram)

Page 28 — Input power Jack (+5V DC)

Page 28 — Overvoltage Protection → +VIN_5V → +VIN_4V2

Page 26 — PMIC PF0100A

+VIN_4V2 → SW1A/B Buck / max 2.5A → +1V375_CORE
+VIN_4V2 → SW1C Buck / max 2A → +1V375_SOC
+VIN_4V2 → SW2 Buck / max 2A → +3V3
+VIN_4V2 → SW3A/B Buck / max 2.5A → +1V5_DDR
+VIN_4V2 → SW4 Buck / max 1A → +0V75_DDR_VTT
+VIN_4V2 → SWBST Boost / max 0.6A → +5V
+3V3 → VGEN1 Ldo / max 0.1A → +1V2_PMIC
+3V3 → VGEN2 Ldo / max 0.25A → +1V8_AUDIO
+3V3 → VGEN3 Ldo / max 0.1A → +2V5
+VIN_4V2 → VGEN4 Ldo / max 0.35A → +3V3_LDO
+VIN_4V2 → VGEN5 Ldo / max 0.1A → +3V0_ALWAYS
VGEN6 Ldo / max 0.2A
LICELL
+VIN_4V2 → VSNVS → +3V0_VSNVS

+VIN_4V2 → Page 27 +1V375 CPU SOC (Optional) → +1V375_SOC
+VIN_4V2 → Page 27 +3V3 (Optional) → +3V3_HDR
+VIN_4V2 → Page 15 +1V2_ETH → +1V2_REG
+3V3

Pages 4 - 13 — NXP i.MX6 CPU (up to 1.2GHz) ARM Cortex A9

Page 3 — DDR3 MEMORIES (up to 4GB DDR3) 32/64bit, DDR3-800/1066 — DDR3
Page 22 — EEPROM — I2C1
Page 23 — Gyroscope — I2C1
Page 23 — Compass + Accelerometer — I2C1
Page 23 — Temperature Sensor — I2C2
Page 23 — Humidity Sensor — I2C2
Page 23 — Infra Red Receiver — GPIO

USER Button (e.g. RECENT, VOLUME+) — BTN3
USER Button (e.g. BACK, VOLUME-) — BTN2
USER Button (e.g. HOME, WAKE UP...) — BTN1
RESET / POWER Button
USER LED (ORANGE) — +3V3
8x USER LEDs (RED) — +3V3 — 8x USER_LED
4x USER_LED

Page 16 — HDMI (Output) — HDMI
Page 17 — MIPI CSI Camera (Raspberry Pi Compatible) or LVDS Display Connector — LVDS0, CSI (MIPI, differential camera input)
Page 17 — Parallel CSI Camera or Parallel RGB Display Connector — VIDEO INPUT (CSI1, par. camera in., 20bit) OR DISP1 (Parallel LCD display output, 20bit)
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Page 28 — USB OTG (Optional Power Input) → +VIN_5V
Page 19 — USB-A Stacked Connector — USBDN1, USBDN2
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+3V3 → POWER LED (GREEN)
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Page 22 — SPI Switch (Optional) — SPI3
Page 17 — Touch screen Header

http://www.iMX6Rex.com/

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CPU - DDR3, DDR3 MEM

DESIGN NOTE:
When using data bit swapping the low order bit of eachbyte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

ClassName: DRAM_ADDR_CTRL
Net Class

U1C
i.MX6Q - DDR

DRAM_D[63..0]
DRAM_A[15..0]

ClassName: DRAM_BANK0 / Net Class 1
DRAM_D0 AD2 — DRAM_D0
DRAM_D1 AE2 — DRAM_D1
DRAM_D2 AC4 — DRAM_D2
DRAM_D3 AA5 — DRAM_D3
DRAM_D4 AC1 — DRAM_D4
DRAM_D5 AD1 — DRAM_D5
DRAM_D6 AB4 — DRAM_D6
DRAM_D7 AE4 — DRAM_D7
DRAM_DQS0_P DIFF100 AE3 — DRAM_SDQS0
DRAM_DQS0_N DIFF100 AD3 — DRAM_SDQS0
DRAM_DQM0 AC3 — DRAM_DQM0

ClassName: DRAM_BANK1 / Net Class 1
DRAM_D8 AD5 — DRAM_D8
DRAM_D9 AE5 — DRAM_D9
DRAM_D10 AA6 — DRAM_D10
DRAM_D11 AE7 — DRAM_D11
DRAM_D12 AB5 — DRAM_D12
DRAM_D13 AC5 — DRAM_D13
DRAM_D14 AB6 — DRAM_D14
DRAM_D15 AC7 — DRAM_D15
DRAM_DQS1_P DIFF100 AD6 — DRAM_SDQS1
DRAM_DQS1_N DIFF100 AE6 — DRAM_SDQS1
DRAM_DQM1 AC6 — DRAM_DQM1

ClassName: DRAM_BANK2 / Net Class 1
DRAM_D16 AB7 — DRAM_D16
DRAM_D17 AA8 — DRAM_D17
DRAM_D18 AB9 — DRAM_D18
DRAM_D19 Y8 — DRAM_D19
DRAM_D20 Y7 — DRAM_D20
DRAM_D21 Y8 — DRAM_D21
DRAM_D22 AC8 — DRAM_D22
DRAM_D23 AA9 — DRAM_D23
DRAM_DQS2_P DIFF100 AD8 — DRAM_SDQS2
DRAM_DQS2_N DIFF100 AE8 — DRAM_SDQS2
DRAM_DQM2 AB8 — DRAM_DQM2

ClassName: DRAM_BANK3 / Net Class 1
DRAM_D24 AE9 — DRAM_D24
DRAM_D25 Y10 — DRAM_D25
DRAM_D26 AE11 — DRAM_D26
DRAM_D27 AB11 — DRAM_D27
DRAM_D28 AC9 — DRAM_D28
DRAM_D29 AD9 — DRAM_D29
DRAM_D30 AD11 — DRAM_D30
DRAM_D31 AC11 — DRAM_D31
DRAM_DQS3_P DIFF100 AC10 — DRAM_SDQS3
DRAM_DQS3_N DIFF100 AB10 — DRAM_SDQS3
DRAM_DQM3 AE10 — DRAM_DQM3

ClassName: DRAM_BANK4 / Net Class 1
DRAM_D32 AA17 — DRAM_D32
DRAM_D33 AA18 — DRAM_D33
DRAM_D34 AC18 — DRAM_D34
DRAM_D35 AE19 — DRAM_D35
DRAM_D36 Y17 — DRAM_D36
DRAM_D37 Y18 — DRAM_D37
DRAM_D38 AB19 — DRAM_D38
DRAM_D39 AC19 — DRAM_D39
DRAM_DQS4_P DIFF100 AD18 — DRAM_SDQS4
DRAM_DQS4_N DIFF100 AE18 — DRAM_SDQS4
DRAM_DQM4 AB18 — DRAM_DQM4

ClassName: DRAM_BANK5 / Net Class 1
DRAM_D40 Y19 — DRAM_D40
DRAM_D41 AB20 — DRAM_D41
DRAM_D42 AB21 — DRAM_D42
DRAM_D43 AD22 — DRAM_D43
DRAM_D44 Y20 — DRAM_D44
DRAM_D45 AA20 — DRAM_D45
DRAM_D46 AE22 — DRAM_D46
DRAM_D47 AC21 — DRAM_D47
DRAM_DQS5_P DIFF100 AC20 — DRAM_SDQS5
DRAM_DQS5_N DIFF100 AE20 — DRAM_SDQS5
DRAM_DQM5 AC20 — DRAM_DQM5

ClassName: DRAM_BANK6 / Net Class 1
DRAM_D48 AC22 — DRAM_D48
DRAM_D49 AE23 — DRAM_D49
DRAM_D50 AE24 — DRAM_D50
DRAM_D51 AC24 — DRAM_D51
DRAM_D52 AB22 — DRAM_D52
DRAM_D53 AC23 — DRAM_D53
DRAM_D54 AD23 — DRAM_D54
DRAM_D55 AC25 — DRAM_D55
DRAM_DQS6_P DIFF100 AD23 — DRAM_SDQS6
DRAM_DQS6_N DIFF100 AE23 — DRAM_SDQS6
DRAM_DQM6 AD24 — DRAM_DQM6

ClassName: DRAM_BANK7 / Net Class 1
DRAM_D56 AB25 — DRAM_D56
DRAM_D57 AA21 — DRAM_D57
DRAM_D58 Y25 — DRAM_D58
DRAM_D59 Y22 — DRAM_D59
DRAM_D60 AB23 — DRAM_D60
DRAM_D61 AA23 — DRAM_D61
DRAM_D62 Y23 — DRAM_D62
DRAM_D63 W25 — DRAM_D63
DRAM_DQS7_P DIFF100 AA25 — DRAM_SDQS7
DRAM_DQS7_N DIFF100 AA24 — DRAM_SDQS7
DRAM_DQM7 Y21 — DRAM_DQM7

DRAM_A0 AC14 — DRAM_A0
DRAM_A1 AB14 — DRAM_A1
DRAM_A2 AA14 — DRAM_A2
DRAM_A3 Y14 — DRAM_A3
DRAM_A4 W14 — DRAM_A4
DRAM_A5 AE13 — DRAM_A5
DRAM_A6 AC13 — DRAM_A6
DRAM_A7 Y13 — DRAM_A7
DRAM_A8 AB13 — DRAM_A8
DRAM_A9 AE12 — DRAM_A9
DRAM_A10 AA15 — DRAM_A10
DRAM_A11 AC12 — DRAM_A11
DRAM_A12 AD12 — DRAM_A12
DRAM_A13 AC17 — DRAM_A13
DRAM_A14 AA12 — DRAM_A14
DRAM_A15 Y12 — DRAM_A15

DRAM_SDBA0 AC15 — DRAM_SDBA0
DRAM_SDBA1 Y15 — DRAM_SDBA1
DRAM_SDBA2 AB12 — DRAM_SDBA2

DRAM_CS0 Y16 — DRAM_CS0_B
DRAM_CS1 AD17 — (not used)

DRAM_RAS AB15 — DRAM_RAS_B
DRAM_CAS AE16 — DRAM_CAS_B
DRAM_SDWE AB16 — DRAM_WE_B

DRAM_SDCKE0 Y11 — DRAM_SDCKE0
DRAM_SDCKE1 AA11 — (not used)

DRAM_SDODT0 AC16 — DRAM_SDODT0
DRAM_SDODT1 AB17 — (not used)

DRAM_RESET Y6 — DRAM_RESET_B
R7 10k

DRAM_SDCLK_0 AD15 — DIFF100 — DRAM_CLK0_P
DRAM_SDCLK_0 AE15 — DIFF100 — DRAM_CLK0_N
DRAM_SDCLK_1 AD14 — DIFF100 — DRAM_CLK1_P
DRAM_SDCLK_1 AE14 — DIFF100 — DRAM_CLK1_N
NF C327 2p2
NF C328 2p2
Net Class
ClassName: DRAM_SDCLK

+DDR_VREF
C7 100n
DRAM_VREF AC2

ZQPAD AE17 — ZQPAD
R10 240R
+1V5_DDR
R18 T18 U18 V10 V11 V12 V13 V14 V15 V16 V17 V18 V9
NVCC_DRAM_1 … NVCC_DRAM_13
Net Class
ClassName: DRAM_OTHERS

MCIMX6Q5EYM10AC_v.ORX

DESIGN NOTE:
DRAM_SDCKE0 no longer requires external 10 k©resistors to GND to minimize current drain during deep sleep mode (DSM).
We keep the option to stay compatible with old CPU revisions.

U2 / U3 / U4 / U5
4G_DDR3_SDRAM_256MX16
MT41J256M16HA-125:E

+1V5_DDR
VDD1 B2, VDD2 D2, VDD3 G7, VDD4 K2, VDD5 K8, VDD6 N1, VDD7 N9, VDD8 R1, VDD9 R9
VDDQ1 A1, VDDQ2 A8, VDDQ3 C1, VDDQ4 C9, VDDQ5 E2, VDDQ6 E9, VDDQ7 F1, VDDQ8 H2, VDDQ9 H9

DRAM_A[15..0] → A0 N3, A1 P7, A2 P3, A3 N2, A4 P8, A5 P2, A6 R8, A7 R2, A8 T8, A9 R3, A10 L7, A11 R7, A12/BC N7, A13 T3, BA0 M2, BA1 N8, BA2 M3
DRAM_CS0_B L2 — CS
DRAM_RAS_B J3 — RAS
DRAM_CAS_B K3 — CAS
DRAM_WE_B L3 — WE
DRAM_CLK0_P J7 — CK
DRAM_CLK0_N K7 — CK
DRAM_SDCKE0 K9 — CKE
DRAM_RESET_B T2 — RESET
DRAM0_ZQ L8 — ZQ
DRAM_SDODT0 K1 — ODT
VREFCA M8, VREFDQ H1
DRAM_DQM0 E7, DRAM_DQM1 D3 — LDM, UDM

DRAM_D[63..0] → DQ0 E3, DQ1 F7, DQ2 F2, DQ3 F8, DQ4 H3, DQ5 H8, DQ6 G2, DQ7 H7, DQ8 D7, DQ9 C3, DQ10 C8, DQ11 C2, DQ12 A7, DQ13 A2, DQ14 B8, DQ15 A3
LDQS F3, LDQS G3 — DRAM_DQS0_P, DRAM_DQS0_N
UDQS C7, UDQS B7 — DRAM_DQS1_P, DRAM_DQS1_N

NC_J1 J1, NC_J9 J9, NC_L1 L1, NC_L9 L9, NC_M7 T7, A14 — DRAM0_ZQ1, DRAM_A15, DRAM_A14

R4 240R, R6 10k, +DDR_VREF
C3 220n, C4 220n

U3: R306 240R, R5 240R, +DDR_VREF, C5 220n, C6 220n; DRAM1_ZQ1; R307 240R
U4: R8 240R, +DDR_VREF, C8 220n, C9 220n; DRAM2_ZQ1; R9 240R
U5: R308 240R, +DDR_VREF, C10 220n, C11 220n; DRAM3_ZQ1; R309 240R

DESIGN NOTE:
DDR VREF voltage is generated by PMIC controller by default. To use resistor divider instead, do not fit R345 and fit R245 & R274.

+1V5_DDR
R245 0R, R274 0R
NF C392 100n, NF C393 100n
+DDR_VREF
C19 10u

DESIGN NOTE:
When iMX6 Solo Procesor will be used (32-bit data bus), do not fit U4 and U5.

DESIGN NOTE:
Freescale measurement shows maximum current drawn from +1V5_DDR by CPU and memories up to 1400mA.

+1V5_DDR
C27 22u, C28 22u, C29 22u, C31 22u, C32 22u, C33 22u
C1 220n, C2 220n, C12 220n, C21 220n, C22 220n, C23 220n, C24 220n, C25 220n, C26 220n, C30 220n
C34 220n, C35 220n, C36 220n, C37 220n, C38 220n, C39 220n, C40 220n, C41 220n, C42 220n, C43 220n
C44 220n, C45 220n, C46 220n, C47 220n, C48 220n, C49 220n, C50 220n, C51 220n, C52 220n, C53 220n
C54 220n, C55 220n, C56 220n, C57 220n, C58 220n, C59 220n, C60 220n, C203 220n, C204 220n, C205 220n

Address, command and control signal termination: Place at the end of each signal

DRAM_A[15..0] → +0V75_DDR_VTT
DRAM_A0 47R R1, DRAM_A1 47R R3, DRAM_A2 47R R12, DRAM_A3 47R R31, DRAM_A4 47R R38, DRAM_A5 47R R40, DRAM_A6 47R R44, DRAM_A7 47R R50, DRAM_A8 47R R72, DRAM_A9 47R R79, DRAM_A10 47R R103, DRAM_A11 47R R105, DRAM_A12 47R R106, DRAM_A13 47R R107, DRAM_A14 47R R108, DRAM_A15 47R R111

+1V5_DDR
C13 100n, C14 100n, C15 100n, C16 100n, C17 100n, C18 100n, C20 22u
C229 100n, C277 100n, C297 100n, C305 100n, C306 100n, C308 100n, C321 22u

DRAM_SDBA0 47R R2, DRAM_SDBA1 47R R11, DRAM_SDBA2 47R R22, DRAM_RAS_B 47R R34, DRAM_CAS_B 47R R39, DRAM_WE_B 47R R42, DRAM_CS0_B 47R R45, DRAM_SDCKE0 47R R66, DRAM_SDODT0 47R R77

+1V5_DDR
C74 100n, C85 100n, C86 100n, C206 100n
C317 100n, C318 100n, C319 100n, C320 100n

Clock termination: Place at end of each CLK pair

DRAM_CLK0_N 49R9 R112 — DRAM_CLK0_T_CAP — C322 100n — +1V5_DDR
DRAM_CLK0_P 49R9 R253
DRAM_CLK1_N 49R9 R113 — DRAM_CLK1_T_CAP — C323 100n — +1V5_DDR
DRAM_CLK1_P 49R9 R256

DESIGN NOTE:
8Gb DDR3 memories with second ZQ pad are supported - fit resistors R306-R309.

DESIGN NOTE:
Using bit swapping for DATA bus to allow easy pcb routing.
When swapping the whole bytes, remember to move the DQMx, DQSx, and DQSx_B signals.

DESIGN NOTE:
DDR3 termination max. current calculation:
I_one = Vtt / R_vtt = 0.75 V / 47 Ohm = 16 mA
I_vtt = I_one * number of res = 16 mA * 25 = 0.4 A

LAYOUT NOTE:
Maintain 50 Ohm impedance for single ended tracks.

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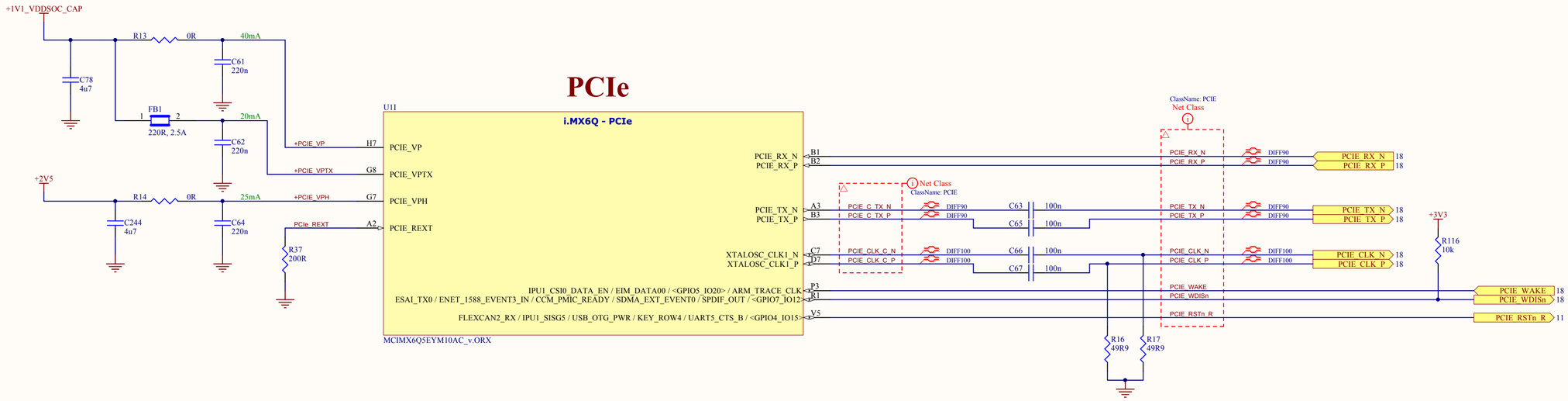
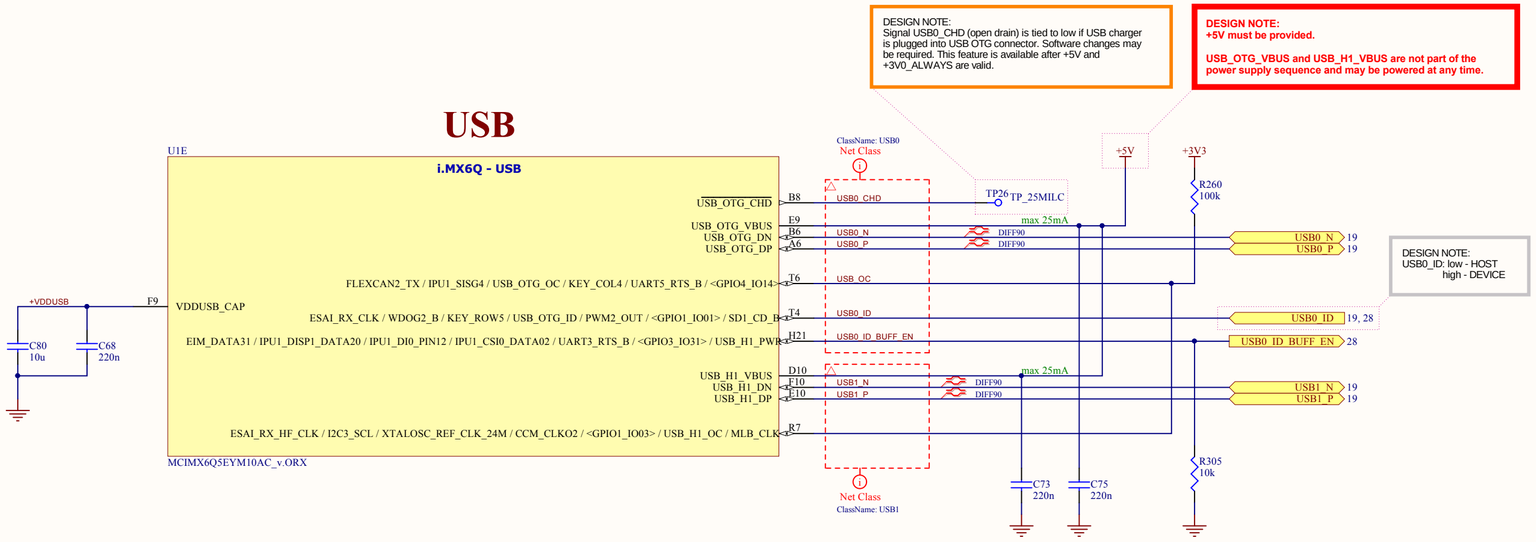
CPU - PCIE, USB

PCIe



USB



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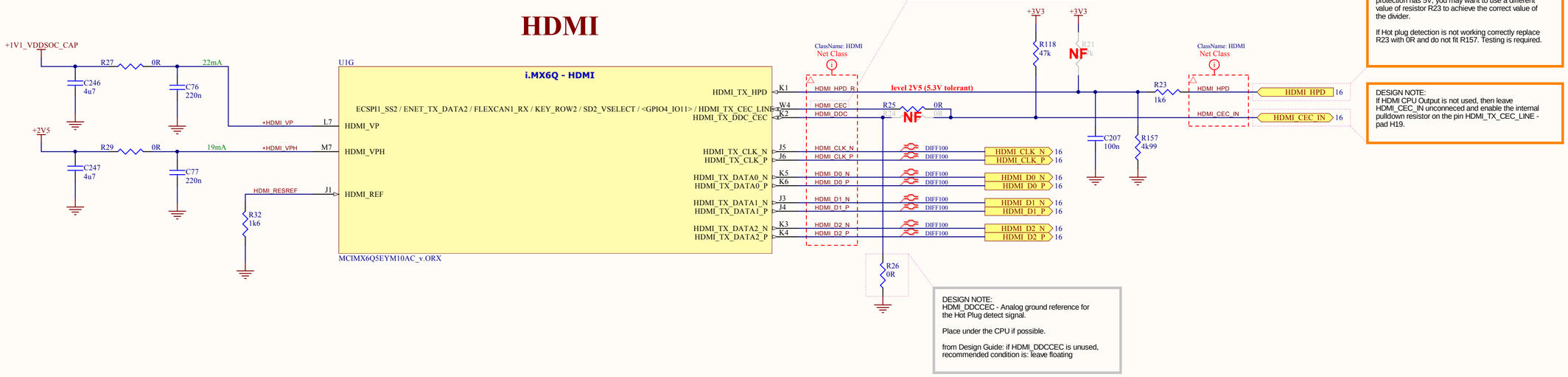
CPU - HDMI, LVDS

HDMI



DESIGN NOTE:
HDMI_CEC signal has been moved to a new pin - software change is required. After reset this pin is output low by default.

DESIGN NOTE:
Resistors R23, R157 are used as a divider to get a correct voltage on CPU HPD pin. This divider may not be required, as it looks like the HDMI_TX_HPD should be 5V tollerant, but it's not 100% clear from the documentation:

HPD level:
High: 2 - 5.3V
Low: 0-0.8V

Divider calculation:
HDMI_HPD_R level = HDMI_HPD level * R157 / (R23+R157) = 3.3 * 4k99 / (4k99+1k6) = 2.5V

If the HDMI_HPD signal coming from the HDMI protection has 5V, you may want to use a different value of resistor R23 to achieve the correct value of the divider.

If Hot plug detection is not working correctly replace R23 with 0R and do not fit R157. Testing is required.

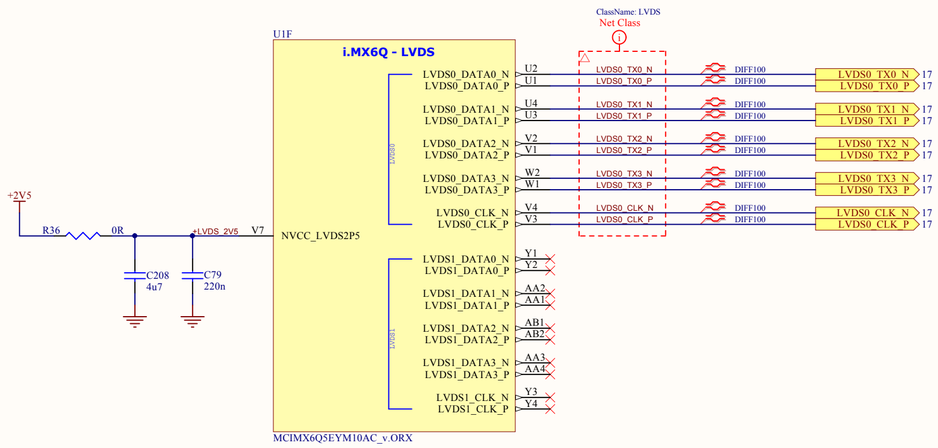
DESIGN NOTE:
If HDMI CPU Output is not used, then leave HDMI_CEC_IN unconneced and enable the internal pulldown resistor on the pin HDMI_TX_CEC_LINE - pad H19.

DESIGN NOTE:
HDMI_DDCCEC - Analog ground reference for the Hot Plug detect signal.

Place under the CPU if possible.

from Design Guide: if HDMI_DDCCEC is unused, recommended condition is: leave floating

LVDS



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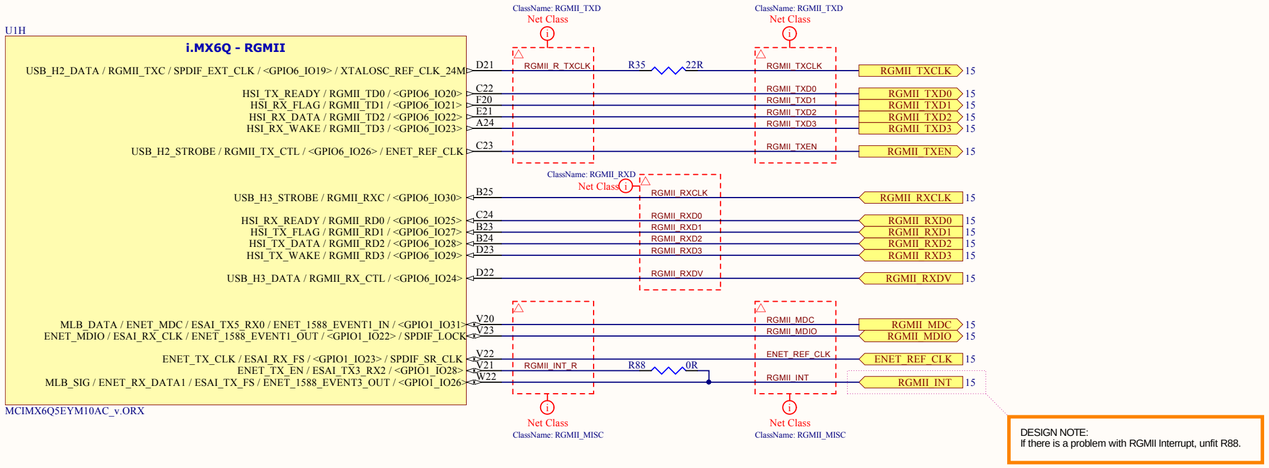
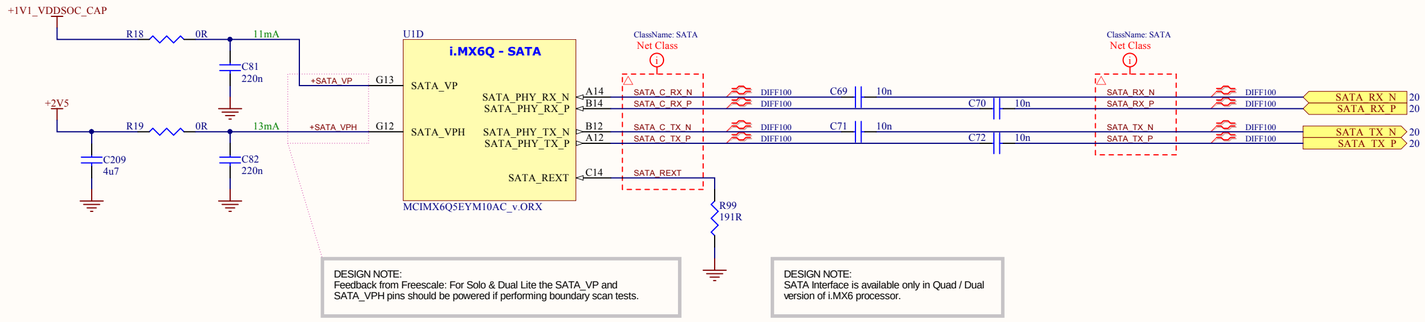
CPU - ETHERNET, SATA

ETHERNET



SATA



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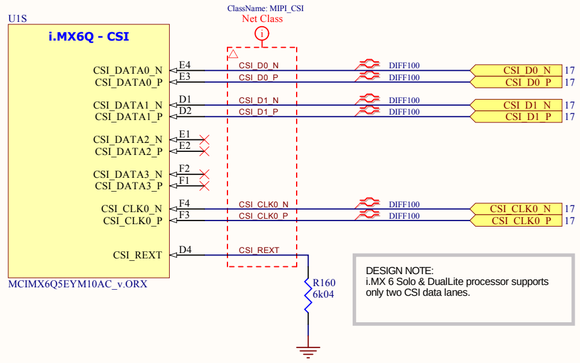
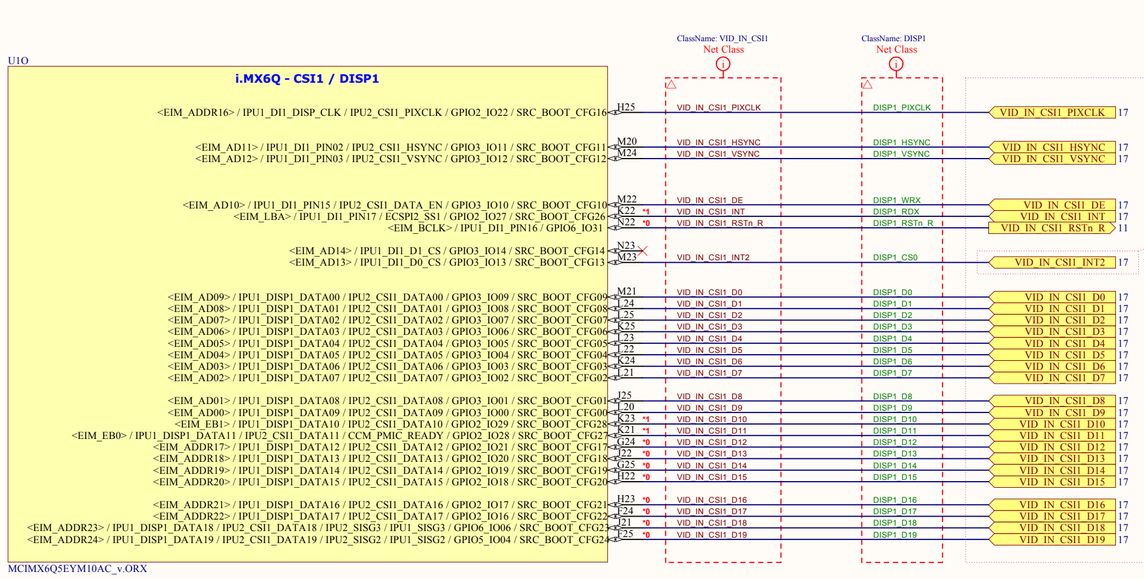
CPU - CSI, DISP

Serial Camera Interface CSI



Parallel Camera Interface CSI1 / DISP1



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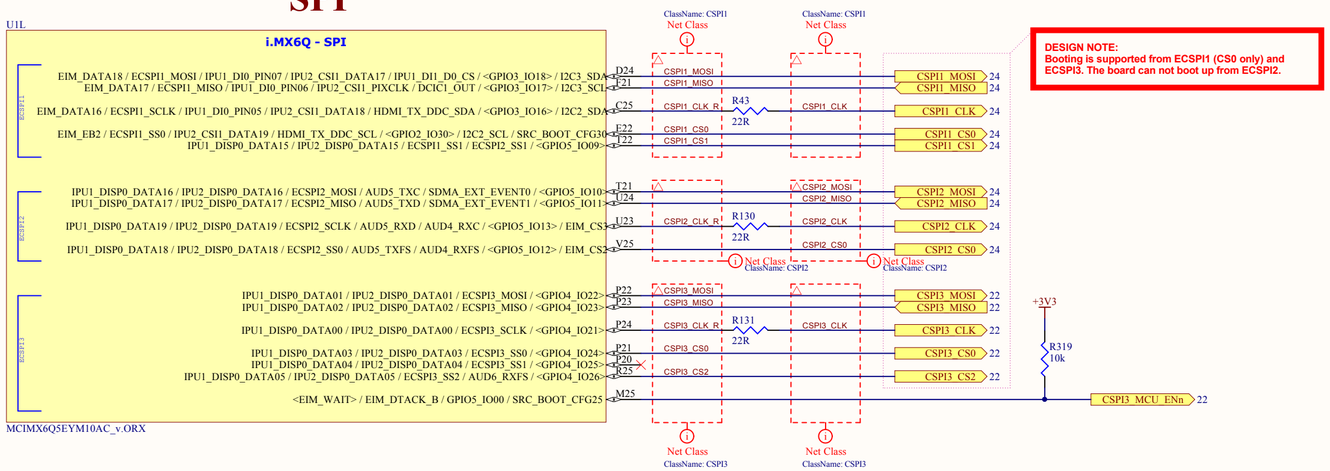
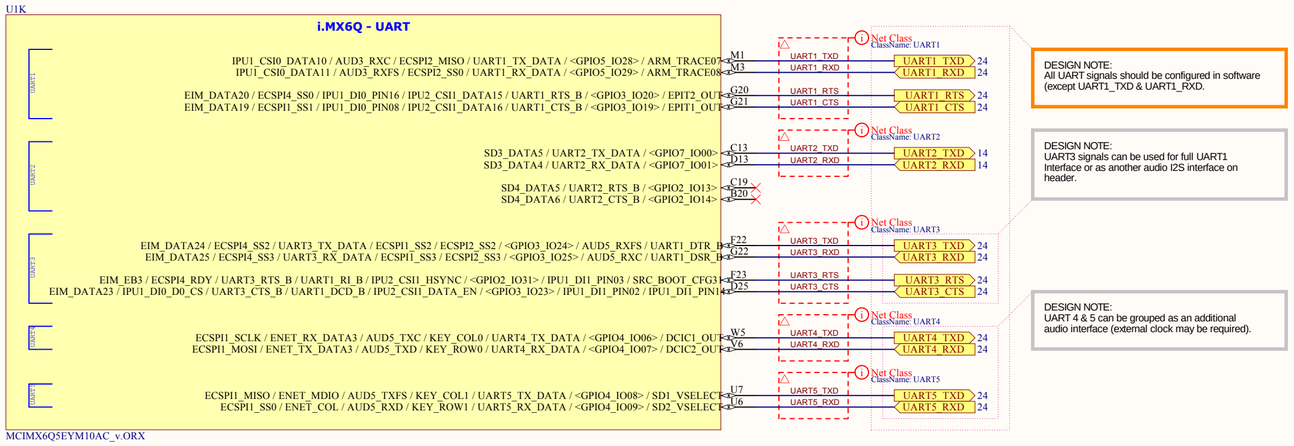
CPU - SPI, UART

SPI



DESIGN NOTE:
Booting is supported from ECSPI1 (CS0 only) and ECSPI3. The board can not boot up from ECSPI2.

UART



DESIGN NOTE:
All UART signals should be configured in software (except UART1_TXD & UART1_RXD.

DESIGN NOTE:
UART3 signals can be used for full UART1 Interface or as another audio I2S interface on header.

DESIGN NOTE:
UART 4 & 5 can be grouped as an additional audio interface (external clock may be required).

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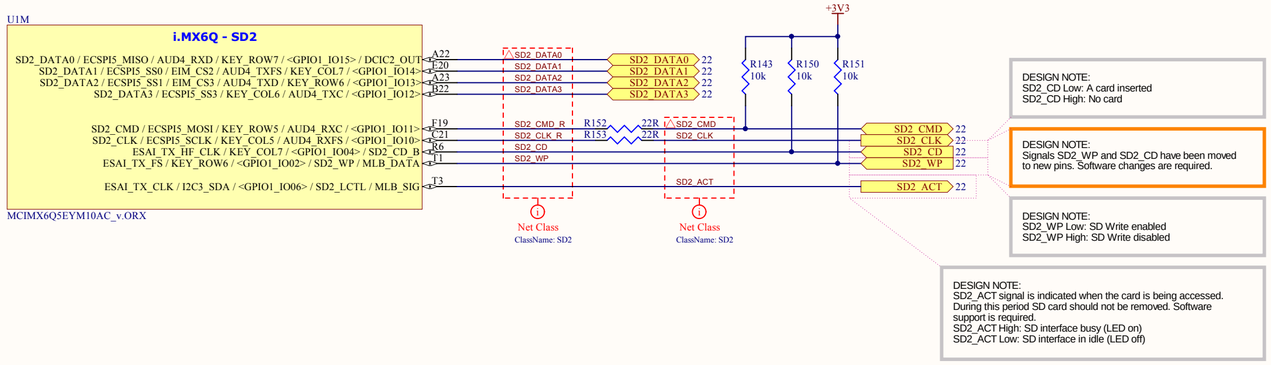
CPU - SD CARD, AUDIO, I2C, CAN

SD Card



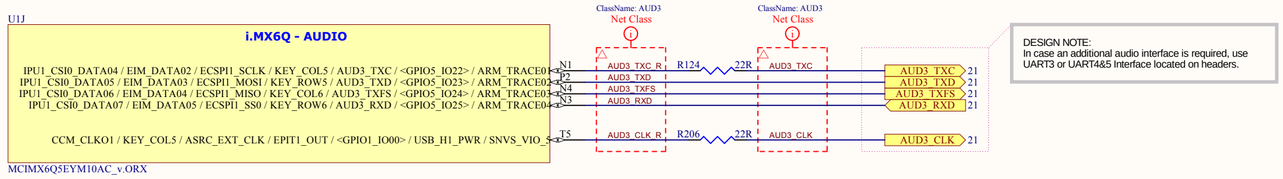
DESIGN NOTE:
SD2_CD Low: A card inserted
SD2_CD High: No card

DESIGN NOTE:
Signals SD2_WP and SD2_CD have been moved to new pins. Software changes are required.

DESIGN NOTE:
SD2_WP Low: SD Write enabled
SD2_WP High: SD Write disabled

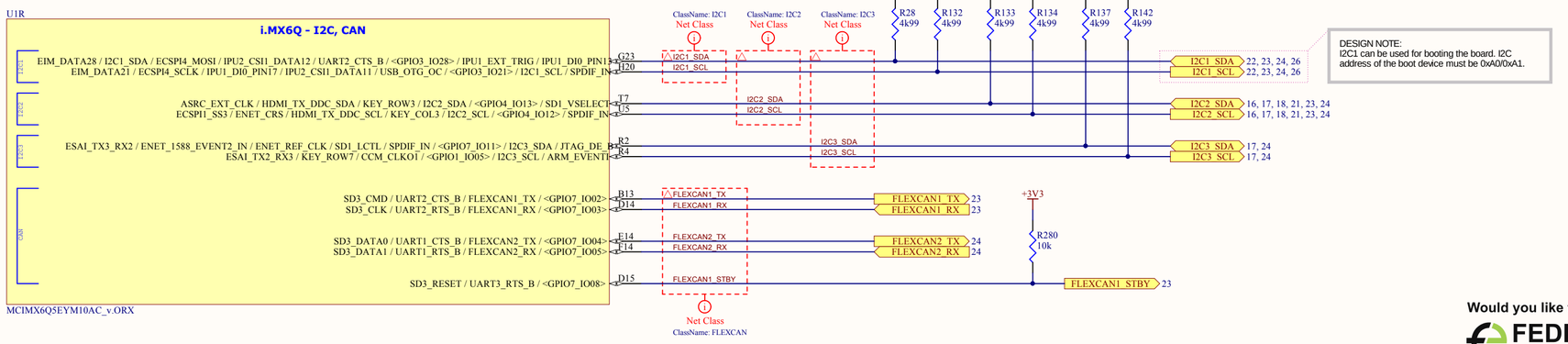
DESIGN NOTE:
SD2_ACT signal is indicated when the card is being accessed. During this period SD card should not be removed. Software support is required.
SD2_ACT High: SD interface busy (LED on)
SD2_ACT Low: SD interface in idle (LED off)

AUDIO



DESIGN NOTE:
In case an additional audio interface is required, use UART3 or UART4&5 Interface located on headers.

I2C, CAN



DESIGN NOTE:
I2C1 can be used for booting the board. I2C address of the boot device must be 0xA0/0xA1.

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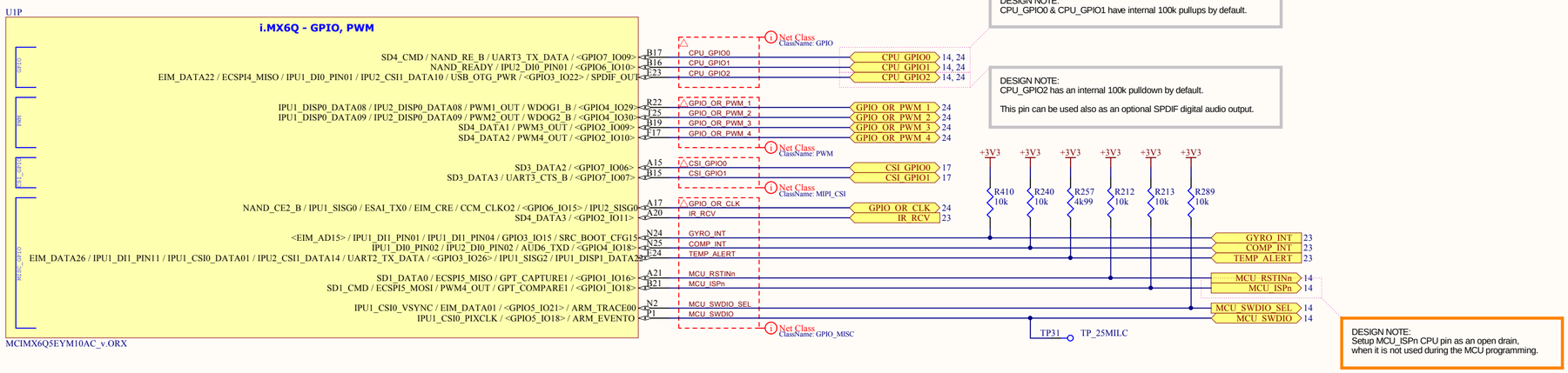
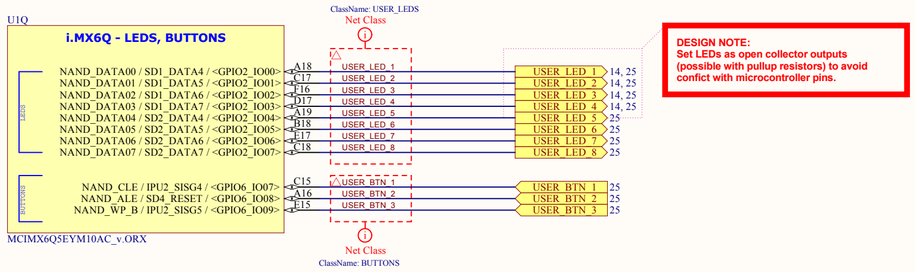
CPU - GPIO, PWM, LEDS, BUTTONS

GPIO, PWM



LEDS, BUTTONS



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CPU - JTAG, CONTROL

CONTROL

U1A

i.MX6Q - CONTROL

MCIMX6Q5EYM10AC_v.ORX

+3V0_ALWAYS

R48 10k

TP3 TP_25MILC

DESIGN NOTE:
PMIC_STBY_REQ_CPU enters and exits PMIC standby:
0->1 = enter standby
1->0 = wake-up from standby

DESIGN NOTE:
PMIC_ON_REQ:
1 or high Z = ON
0 = OFF

DESIGN NOTE:
WD_OUT configure in software first.

DESIGN NOTE:
Resistor R20 from CPU_XTALI to GND is required to correct a known 24MHz slow starting issue present on some i.MX6 part. Please refer to the i.MX6 Processor Errata, issue # ERR005777 for more details.

DESIGN NOTE:
Be careful, some pins are connected to 3.0V ALWAYS

DESIGN NOTE:
RSTOUTn, VID_IN_CSI1_RSTn and PCIE_RSTn:
ALWAYS FIT ONLY ONE OF THE 0R Resistors (e.g. R51 or R70, R179 or R178, R170 or R158). Wrong configuration may prevent your board from booting. If manual reset is use, be sure you setup these pins correctly in software.

DESIGN NOTE:
RSTOUTn is setup as a Low Output signal after reset. Software support is required.

DESIGN NOTE:
User LED can be controlled using PWM output.

DESIGN NOTE:
Board variant pins can be used to detect a specific HW version of the iMX6 OpenRex board.

DESIGN NOTE:
BOARD_ID_1 signal is used to detect the board. This way a generic software can identify the board and load a specific configuration.

Board ID configuration:

	Rex	TinyRex	OpenRex
- GPIO5_IO16:	1	0	1
- GPIO5_IO17:	1	1	0
- GPIO1_IO24:	1	1	1

DESIGN NOTE:
Default boot mode: 00 (eFuses).

BOOT MODE [1:0]:
00 Boot from fuses
01 Serial downloader
10 Boot from board settings
11 Reserved

DESIGN NOTE:
Tamper will not be used.

DESIGN NOTE:
Test mode only for factory use.

From Design Guide: TEST_MODE pull down internally - external not required

DESIGN NOTE:
Leave open to boot from eFuses, short to boot from USB OTG.

DESIGN NOTE:
JP2 default:
Unfit Link to boot from eFuses

RESET

DESIGN NOTE:
Fit R177 and do not fit R333 when +3V3 optional source is not used.

POK_1V375_OPT is designed to tie low the POK_SYS if voltage from optional source is not valid. R351 does not depend on the resistors R177 or R333.

DESIGN NOTE:
CT 100nF = 0.6s RESET Delay

DESIGN NOTE:
MR (signal POK_SYS) pin of voltage monitor has an internal pullup resistor connected to +3V0_ALWAYS.

DESIGN NOTE:
If testing shows that reset controller U31 is not required, it can be bypassed with R350.

DESIGN NOTE:
When RGMII_RSTn is controlled by GPIO and also by POR (D1 and R166 both fitted), setup RGMII_RSTn_R as an open drain signal. If it is not used as open drain, it can prevent CPU from booting.

DESIGN NOTE:
If RSTOUTn, VID_IN_CSI1_RSTn, PCIE_RSTn and RGMII_RSTn are controlled by processor GPIOs, do not forget to support them in software first. They can be connected to the POR (while disconnected them from GPIOs) to reset peripherals. Set them as an open drain by default.

BE AWARE!
RGMII_RSTn_R is HIGH after reset.

JTAG

DESIGN NOTE:
from Design Guide: JTAG_MOD use pulldown 1k or tie to GND

DESIGN NOTE:
From Design Guide:
Do not use external PU/PD on JTAG_TDO.

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CPU - POWER

U1B

i.MX6Q - POWER

+1V375_CORE — 2200mA

VDDARM_IN_1 H14, VDDARM_IN_2 J14, VDDARM_IN_3 K14, VDDARM_IN_4 L14, VDDARM_IN_5 M14, VDDARM_IN_6 N14, VDDARM_IN_7 P14, VDDARM_IN_8 R14

C90 220n, C91 220n, C92 220n, C93 220n, C94 220n, C95 220n, C96 22u

DESIGN NOTE:
The maximum listed currents in iMX6 Datasheets are 3920mA (VDD_ARM_IN) and 1890mA (VDD_SOC_IN). However, the real Freescale measurements shows maximum currents 1625 / 1250mA (see AN4509 Dual/Quad Power Consumption Measurement, page 21)

VDDARM23_IN_1 K9, VDDARM23_IN_2 L9, VDDARM23_IN_3 M9, VDDARM23_IN_4 N9, VDDARM23_IN_5 P9, VDDARM23_IN_6 R9, VDDARM23_IN_7 T9, VDDARM23_IN_8 U9

C107 220n, C108 220n, C109 220n, C110 220n, C111 22u

+1V375_SOC — 1600mA (up to 3390mA for i.MX6DQPlus)

VDDSOC_IN_1 H16, VDDSOC_IN_2 J16, VDDSOC_IN_3 K16, VDDSOC_IN_4 L16, VDDSOC_IN_5 M16, VDDSOC_IN_6 N16, VDDSOC_IN_7 P16, VDDSOC_IN_8 R16, VDDSOC_IN_9 T16, VDDSOC_IN_10 U16

C119 220n, C120 220n, C121 220n, C122 220n, C123 220n, C124 220n, C125 220n, C126 220n, C127 22u, C128 22u, C129 22u

+3V0_ALWAYS — 100mA (max 125mA)*

VDDHIGH_IN_1 H9, VDDHIGH_IN_2 J9

C136 220n, C137 22u

275uA (peak 1mA)

VDD_SNVS_IN G11

C142 220n

DESIGN NOTE:
* The maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs.

GND_1 A13, GND_2 A25, GND_3 A4, GND_4 A8, GND_5 AA10, GND_6 AA13, GND_7 AA16, GND_8 AA19, GND_9 AA22, GND_10 AA7, GND_11 AB24, GND_12 AB3, GND_13 AD10, GND_14 AD13, GND_15 AD16, GND_16 AD19, GND_17 AD22, GND_18 AD4, GND_19 AD7, GND_20 AE1, GND_21 AE25, GND_22 B4, GND_23 C1, GND_24 C10, GND_25 C4, GND_26 C6, GND_27 D3, GND_28 D6, GND_29 D8, GND_30 E5, GND_31 E6, GND_32 E7, GND_33 F5, GND_34 F6, GND_35 F7, GND_36 F8, GND_37 G10, GND_38 G19, GND_39 G3, GND_40 H12, GND_41 H15, GND_42 H18, GND_43 H8, GND_44 J12, GND_45 J15, GND_46 J18, GND_47 J2, GND_48 J8, GND_49 K10, GND_50 K12, GND_51 K15, GND_52 K18, GND_53 K8, GND_54 L10, GND_55 L12, GND_56 L15, GND_57 L18, GND_58 L2, GND_59 L5, GND_60 L8, GND_61 M10, GND_62 M12, GND_63 M15, GND_64 M18, GND_65 M8, GND_66 N10, GND_67 N15, GND_68 N18, GND_69 N8, GND_70 P10, GND_71 P12, GND_72 P15, GND_73 P18, GND_74 P8, GND_75 R12, GND_76 R15, GND_77 R17, GND_78 R8, GND_79 T11

DESIGN NOTE:
i.MX6 power domains under-BGA decoupling (belongs to the CPU pins on page 4).

+1V5_DDR

C157 220n, C158 220n, C159 220n, C160 220n, C161 220n, C162 220n

C167 220n, C168 220n, C169 220n, C170 220n, C171 220n, C172 22u, C173 22u

MCIMX6Q5EYM10AC_v.ORX

DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo Lite processors. (see more info in AN4397, page 7)

+1V2_VDD_ARM_CAP

VDDARM_CAP_1 H13, VDDARM_CAP_2 J13, VDDARM_CAP_3 K13, VDDARM_CAP_4 L13, VDDARM_CAP_5 M13, VDDARM_CAP_6 N13, VDDARM_CAP_7 P13, VDDARM_CAP_8 R13

C97 220n, C98 220n, C99 220n, C100 220n, C101 22u

VDDARM23_CAP_1 H11, VDDARM23_CAP_2 J11, VDDARM23_CAP_3 K11, VDDARM23_CAP_4 L11, VDDARM23_CAP_5 M11, VDDARM23_CAP_6 N11, VDDARM23_CAP_7 P11, VDDARM23_CAP_8 R11

C102 220n, C103 220n, C104 220n, C105 220n, C106 22u

DESIGN NOTE:
The *_CAP signals should not be powered externally. These signals are used for internal LDO or LDO bypass operation only.

+1V1_VDDSOC_CAP

VDDSOC_CAP_1 R10, VDDSOC_CAP_2 T10, VDDSOC_CAP_3 T13, VDDSOC_CAP_4 T14, VDDSOC_CAP_5 U10, VDDSOC_CAP_6 U13, VDDSOC_CAP_7 U14

C112 220n, C113 220n, C114 220n, C115 220n, C116 220n, C117 220n, C118 22u

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails are placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

+VDDPU

VDDPU_CAP_1 H17, VDDPU_CAP_2 J17, VDDPU_CAP_3 K17, VDDPU_CAP_4 L17, VDDPU_CAP_5 M17, VDDPU_CAP_6 N17, VDDPU_CAP_7 P17

C130 220n, C131 220n, C132 220n, C133 220n, C134 220n, C135 22u

VDD_CACHE_CAP N12 — {NVCC_CACHE_POWER}

C138 220n

VDDHIGH_CAP_1 H10, VDDHIGH_CAP_2 J10 — +2V5_VDDHIGH_VPH

C139 10n, C140 220n, C141 22u

VDD_SNVS_CAP G9 — +VDD_SNVS_CAP

+3V3 — C143 220n, C144 220n

NVCC_LCD P19

NVCC_CSI N7 — +NVCC_CSI

NVCC_MIPI K7 — +NVCC_MIPI

DESIGN NOTE:
+NVCC_EIM[2:0] must be connected to the same voltage for Solo / Dual Lite compatibility.

NVCC_EIM0 K19, NVCC_EIM1 L19, NVCC_EIM2 M19

+3V3 — C166 220n, C146 220n, C147 22u, C148 22u

NVCC_ENET R19 — +NVCC_ENET

+1V1_NVCC_PLL_OUT

NVCC_GPIO P7

NVCC_PLL_OUT E8 — +2V5 — R80 0R — C150 220n, C151 22u

NVCC_RGMII G18 — +NVCC_RGMII — +3V3 — C152 220n, C153 220n, C154 220n

DESIGN NOTE:
+NVCC_RGMII connected to 2V5 for RGMII 2V5 operation.

NVCC_SD1 G16

NVCC_SD2 G17 — +3V3 — C163 220n

NVCC_SD3 G14 — +3V3 — C164 220n

NVCC_NANDF G15 — +3V3 — C165 220n

NVCC_JTAG J7 — +3V3 — C174 220n

GPANAIO C8, FA_ANA A5, VDD_FA B5

DESIGN NOTE:
design guide:
- GPANAIO must be left not connected
- VDD_FA and FA_ANA should be tied to GND.

GND_80 T12, GND_81 T15, GND_82 T17, GND_83 T19, GND_84 T8, GND_85 U11, GND_86 U12, GND_87 U15, GND_88 U17, GND_89 U8, GND_90 U19, GND_91 V8, GND_92 V19, GND_93 W3, GND_94 W7, GND_95 W8, GND_96 W9, GND_97 W10, GND_98 W11, GND_99 W12, GND_100 W13, GND_101 W15, GND_102 W16, GND_103 W17, GND_104 W18, GND_105 W19, GND_106 Y5, GND_107 Y24

DESIGN NOTE:
+NVCC_ENET connected to 2V5 as we are using 2V5 PHY.

+NVCC_CSI — +3V3 — R76 0R — C145 220n

+NVCC_MIPI — +2V5 — R78 0R — C149 220n

+NVCC_ENET — +2V5 — R74 0R — C155 220n, C156 22u

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CPU - UNUSED PINS

MISC

U1U

i.MX6Q - UNUSED

SD1_DATA3 / ECSPI5_SS2 / GPT_COMPARE3 / PWM1_OUT / WDOG2_B / <GPIO1_IO21> / WDOG2_RESET_B_DEB — F18
SD1_DATA1 / ECSPI5_SS0 / PWM3_OUT / GPT_CAPTURE2 / <GPIO1_IO17> — C20
SD1_CLK / ECSPI5_SCLK / GPT_CLKIN / <GPIO1_IO20> — D20

SD3_DATA6 / UART1_RX_DATA / <GPIO6_IO18> — E13
SD3_DATA7 / UART1_TX_DATA / <GPIO6_IO17> — F13

SD4_DATA0 / NAND_DQS / <GPIO2_IO08> — D18
SD4_DATA4 / UART2_RX_DATA / <GPIO2_IO12> — E18
SD4_DATA7 / UART2_TX_DATA / <GPIO2_IO15> — D19
SD4_CLK / NAND_WE_B / UART3_RX_DATA / <GPIO7_IO10> — E16

NAND_CE0_B / <GPIO6_IO11> — F15
NAND_CE1_B / SD4_VSELECT / SD3_VSELECT / <GPIO6_IO14> — C16
NAND_CE3_B / IPU1_SISG1 / ESAI_TX1 / EIM_ADDR26 / <GPIO6_IO16> / IPU2_SISG1 — D16

ECSPI1_SS1 / ENET_RX_DATA2 / FLEXCAN1_TX / KEY_COL2 / ENET_MDC / <GPIO4_IO10> / USB_H1_PWR_CTL_WAKE — W6

ESAI_TX4_RX1 / ECSPI5_RDY / EPIT1_OUT / FLEXCAN1_TX / UART2_TX_DATA / <GPIO1_IO07> / SPDIF_LOCK / USB_OTG_HOST_MOD — R3
ESAI_TX5_RX0 / XTALOSC_REF_CLK_32K / EPIT2_OUT / FLEXCAN1_RX / UART2_RX_DATA / <GPIO1_IO08> / SPDIF_SR_CLK / USB_OTG_PWR_CTL_WAKE — R5

IPU1_DISP0_DATA11 / IPU2_DISP0_DATA11 / <GPIO5_IO05> — T23
IPU1_DISP0_DATA20 / IPU2_DISP0_DATA20 / ECSPI1_SCLK / AUD4_TXC / <GPIO5_IO14> — U22
IPU1_DISP0_DATA21 / IPU2_DISP0_DATA21 / ECSPI1_MOSI / AUD4_TXD / <GPIO5_IO15> — T20

IPU1_DI0_PIN15 / IPU2_DI0_PIN15 / AUD6_TXC / <GPIO4_IO17> — N21
IPU1_DI0_PIN03 / IPU2_DI0_PIN03 / AUD6_TXFS / <GPIO4_IO19> — N20

<EIM_CS1> / IPU1_DI1_PIN06 / ECSPI2_MOSI / GPIO2_IO24 — J23
<EIM_OE> / IPU1_DI1_PIN07 / ECSPI2_MISO / GPIO2_IO25 — J24
<EIM_CS0> / IPU1_DI1_PIN05 / ECSPI2_SCLK / GPIO2_IO23 — H24
<EIM_RW> / IPU1_DI1_PIN08 / ECSPI2_SS0 / GPIO2_IO26 / SRC_BOOT_CFG29 — K20

EIM_DATA29 / IPU1_DI1_PIN15 / ECSPI4_SS0 / UART2_RTS_B / <GPIO3_IO29> / IPU2_CSI1_VSYNC / IPU1_DI0_PIN14 — J19
EIM_DATA30 / IPU1_DISP1_DATA21 / IPU1_DI0_PIN11 / IPU1_CSI0_DATA03 / UART3_CTS_B / <GPIO3_IO30> / USB_H1_OC — J20

IPU1_DI0_DISP_CLK / IPU2_DI0_DISP_CLK / <GPIO4_IO16> — N19
IPU1_DISP0_DATA06 / IPU2_DISP0_DATA06 / ECSPI3_SS3 / AUD6_RXC / <GPIO4_IO27> — R23
IPU1_DISP0_DATA10 / IPU2_DISP0_DATA10 / <GPIO4_IO31> — R21
IPU1_DISP0_DATA13 / IPU2_DISP0_DATA13 / AUD5_RXFS / <GPIO5_IO07> — K20

ENET_RX_DATA0 / ESAI_TX_HF_CLK / SPDIF_OUT / <GPIO1_IO27> — W21
MLB_CLK / ENET_TX_DATA1 / ESAI_TX2_RX3 / ENET_1588_EVENT0_IN / <GPIO1_IO29> — W20
ENET_TX_DATA0 / ESAI_TX4_RX1 / <GPIO1_IO30> — U20

MLB_SIG_N — A9
MLB_SIG_P — B9

MLB_DATA_N — B10
MLB_DATA_P — A10

MLB_CLK_N — A11
MLB_CLK_P — B11

MCIMX6Q5EYM10AC_v.ORX

Parallel Camera Interface CSI0

U1N

i.MX6Q - CSI0

IPU1_CSI0_PIXCLK

IPU1_CSI0_VSYNC
IPU1_CSI0_HSYNC / CCM_CLKO1 / <GPIO5_IO19> / ARM_TRACE_CTL — P4

IPU1_CSI0_DATA_EN
ESAI_TX1 / ENET_RX_CLK / SD3_VSELECT / SDMA_EXT_EVENT1 / ASRC_EXT_CLK / <GPIO7_IO13> / SNVS_VIO_5_CTL — P6
KEY_COL5 / ENET_1588_EVENT0_OUT / SPDIF_OUT / CCM_CLKO1 / ECSPI1_RDY / <GPIO4_IO05> / ENET_TX_ER — P5

EIM_DATA27 / IPU1_DI1_PIN13 / IPU1_CSI0_DATA00 / IPU2_CSI1_DATA13 / UART2_RX_DATA / <GPIO3_IO27> / IPU1_SISG3 / IPU1_DISP1_DATA23 — F25
IPU1_CSI0_DATA01
IPU1_CSI0_DATA02
IPU1_CSI0_DATA03

IPU1_CSI0_DATA04
IPU1_CSI0_DATA05
IPU1_CSI0_DATA06
IPU1_CSI0_DATA07
IPU1_CSI0_DATA08 / EIM_DATA06 / ECSPI2_SCLK / KEY_COL7 / I2C1_SDA / <GPIO5_IO26> / ARM_TRACE05 — N6
IPU1_CSI0_DATA09 / EIM_DATA07 / ECSPI2_MOSI / KEY_ROW7 / I2C1_SCL / <GPIO5_IO27> / ARM_TRACE06 — N5
IPU1_CSI0_DATA10
IPU1_CSI0_DATA11

IPU1_CSI0_DATA12 / EIM_DATA08 / UART4_TX_DATA / <GPIO5_IO30> / ARM_TRACE09 — M2
IPU1_CSI0_DATA13 / EIM_DATA09 / UART4_RX_DATA / <GPIO5_IO31> / ARM_TRACE10 — L1
IPU1_CSI0_DATA14 / EIM_DATA10 / UART5_TX_DATA / <GPIO6_IO00> / ARM_TRACE11 — M4
IPU1_CSI0_DATA15 / EIM_DATA11 / UART5_RX_DATA / <GPIO6_IO01> / ARM_TRACE12 — M5
IPU1_CSI0_DATA16 / EIM_DATA12 / UART4_RTS_B / <GPIO6_IO02> / ARM_TRACE13 — L4
IPU1_CSI0_DATA17 / EIM_DATA13 / UART4_CTS_B / <GPIO6_IO03> / ARM_TRACE14 — L3
IPU1_CSI0_DATA18 / EIM_DATA14 / UART5_RTS_B / <GPIO6_IO04> / ARM_TRACE15 — M6
IPU1_CSI0_DATA19 / EIM_DATA15 / UART5_CTS_B / <GPIO6_IO05> — L6

MCIMX6Q5EYM10AC_v.ORX

Serial Display Interface DSI

U1T

i.MX6Q - DSI

DSI_DATA0_N — G2
DSI_DATA0_P — G1

DSI_DATA1_N — H2
DSI_DATA1_P — H1

DSI_CLK0_N — H3
DSI_CLK0_P — H4

DSI_REXT — G4

MCIMX6Q5EYM10AC_v.ORX

Title: OpenRex		Variant: Production	
Page Contents: [13] - CPU - UNUSED.SchDoc			Checked by
Size:	DWG NO		Revision: V1I1
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MCU

DESIGN NOTE:
When +3V3_LDO is used to supply the MCU, and CPU is turned off or in standy, set MCU pins connected to CPU to low (e.g. use internal pull downs, or Low output value), possibly set them as open drain.

DESIGN NOTE:
LPC13xx uses active pull ups & pull downs (current sources).
Equivalent resistance:
- pull up (condition Vin = 3.3V) from 38k to 220k
- pull down (condition Vin = 5V) from 33k to 500k

DESIGN NOTE:
Disable internal pull up resistors on LPC13xx chip which are connected or shared with CPU.

DESIGN NOTE:
If +3V3_LDO is used to power up MCU, do not forget to set MCU RESET (pin 2) as a GPIO pin, so CPU will not RESET MCU during CPU POWER UP/DOWN sequencing.

DESIGN NOTE:
Serial Wire Debugger signals mux option:
SWCLK - signal CSPI3_CLK
SWDIO - signal MCU_SWDIO
SWO - signal CSPI3_MOSI

DESIGN NOTE:
If need, MCU SPI bus can be found on the header J1. Use these signals: CPU_GPIO0 (MOSI1), ANALOG_IN_2 (MISO1), CPU_GPIO1(SCK1), ANALOG_IN_1 (GPIO as CS1). Before you activate MCU SPI MOSI, don't forget to setup SPI CPU pins as inputs.

UART2 Testpoints

UART2_RXD — TP30 — TP_25MILC
UART2_TXD — TP29 — TP_25MILC

DESIGN NOTE:
Fit FB29 (and do not fit FB30) when the board will support standby mode - the whole board (including CPU) will be turned off except the microcontroller and PMIC controll circuit. PMIC standby mode needs to be setup first.

If standard +3V3 and also standby function is needed, replace beads with 0603 diodes and fit both of them.

DESIGN NOTE:
Alternate parts for MCU chip U6: LPC1315, LPC1316, LPC1317, LPC1345, LPC1346, LPC1347.

DESIGN NOTE:
As default method for programming used ISP handler (fitted R205). If USB handler is used do not fit R205 and fit R148 instead.

DESIGN NOTE:
Analog switch U25 selects signal which will be connected to pin PIO0_15.

Switch control (MCU_SWDIO_SEL state):
High (default) - ANALOG_IN_0 signal
Low - MCU_SWDIO signal

If switch will not be fitted, ANALOG_IN_0 can be bypassed with R282.

DESIGN NOTE:
When pads are configured as ADC inputs, pins are not 5 V tolerant.

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Page Contents:	[14] - MCU.SchDoc		Checked by
Size:	DWG NO		Revision: V111
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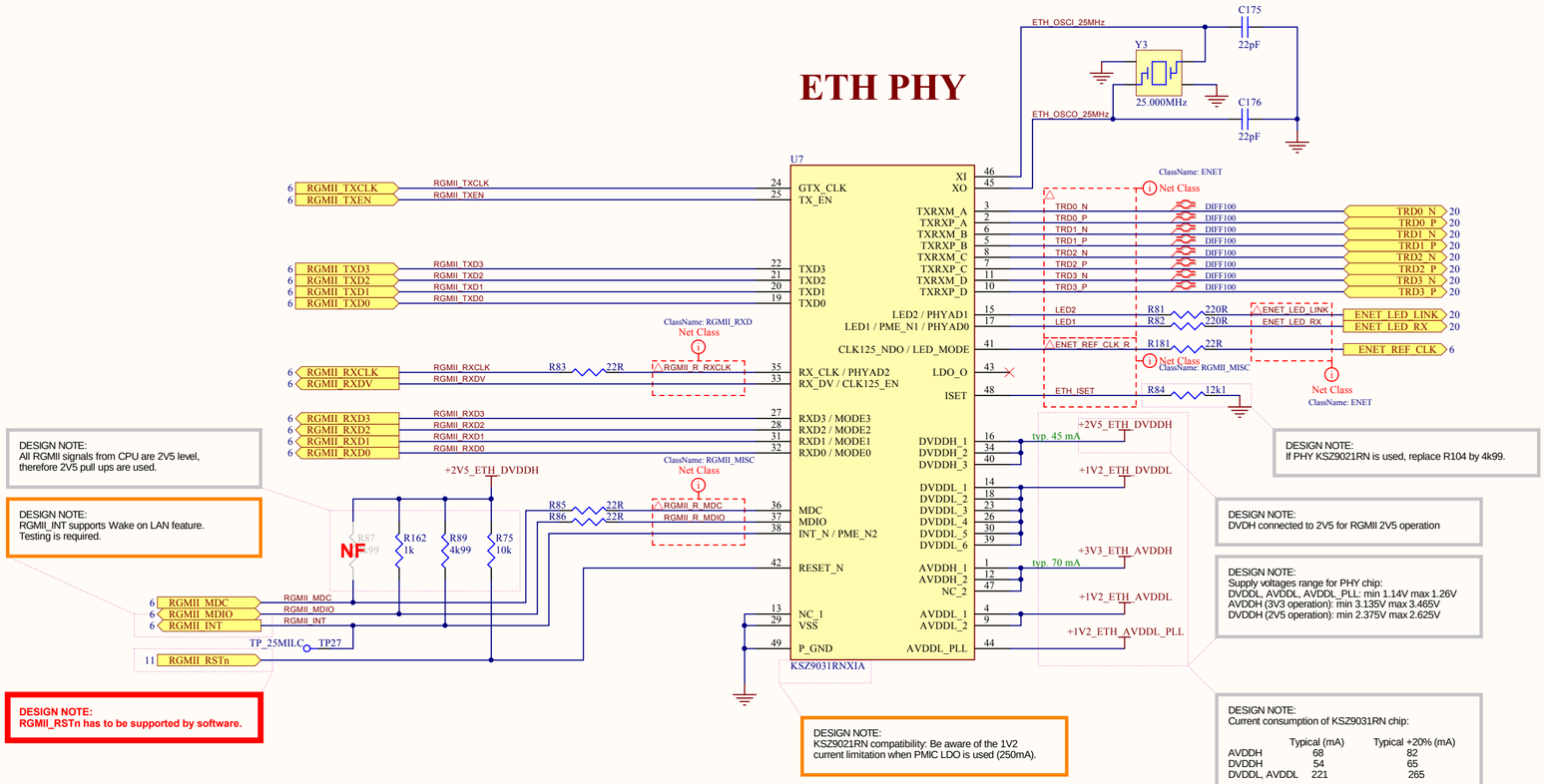
ETHERNET PHY

ETH PHY



DESIGN NOTE:
All RGMII signals from CPU are 2V5 level, therefore 2V5 pull ups are used.

DESIGN NOTE:
RGMII_INT supports Wake on LAN feature. Testing is required.

DESIGN NOTE:
RGMII_RSTn has to be supported by software.

DESIGN NOTE:
If PHY KSZ9021RN is used, replace R104 by 4k99.

DESIGN NOTE:
DVDH connected to 2V5 for RGMII 2V5 operation

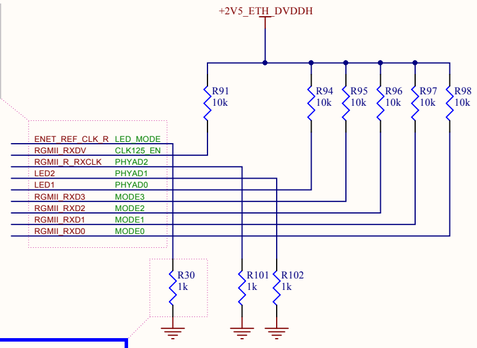
DESIGN NOTE:
Supply voltages range for PHY chip:
DVDDL, AVDDL, AVDDL_PLL: min 1.14V max 1.26V
AVDDH (3V3 operation): min 3.135V max 3.465V
DVDDH (2V5 operation): min 2.375V max 2.625V

DESIGN NOTE:
Current consumption of KSZ9031RN chip:

	Typical (mA)	Typical +20% (mA)
AVDDH	68	82
DVDDH	54	65
DVDDL, AVDDL	221	265

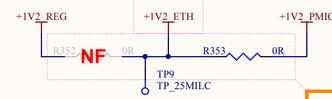
DESIGN NOTE:
KSZ9021RN compatibility. Be aware of the 1V2 current limitation when PMIC LDO is used (250mA).

DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2-0: PHY address 0x1
MODE3-0: RGMII mode (10/100/1000 half/full duplex)
CLK125_EM: ref. clock enable
LED_MODE: tri-color dual mode



LAYOUT NOTE:
Be sure you place R30 directly on the net to minimize stubs.

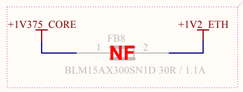
DESIGN NOTE:
+1V2_ETH power rail
+1.2V / Required 250mA



DESIGN NOTE:
+1V2_ETH selection. Fit one of the resistors R352 or R353.

By default, PMIC LDO is selected. If testing shows, that PHY requires higher current, use +1V2_REG source output.

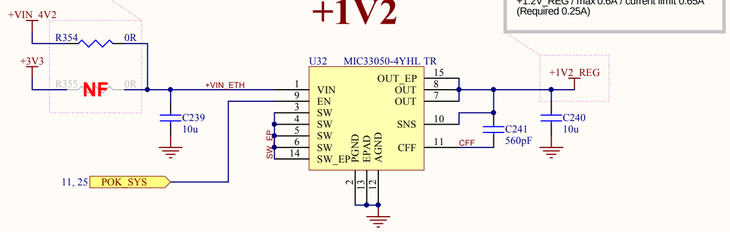
DESIGN NOTE:
Bead for opportunity to connect together +1V2_ETH and +1V375_CORE. Beware: Fit bead FB8 only when supply +1V375_CORE is set to +1V24 and +1V2 is disabled.

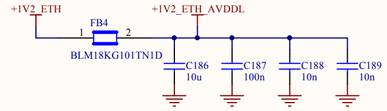


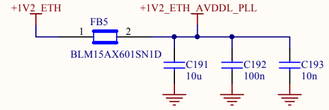
DESIGN NOTE:
Input voltage selection for +1.2V_REG.
Fit only one resistor at a time.

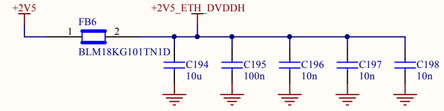
+1V2

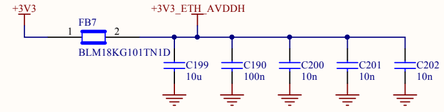
DESIGN NOTE:
+1.2V_REG / max 0.6A / current limit 0.65A (Required 0.25A)











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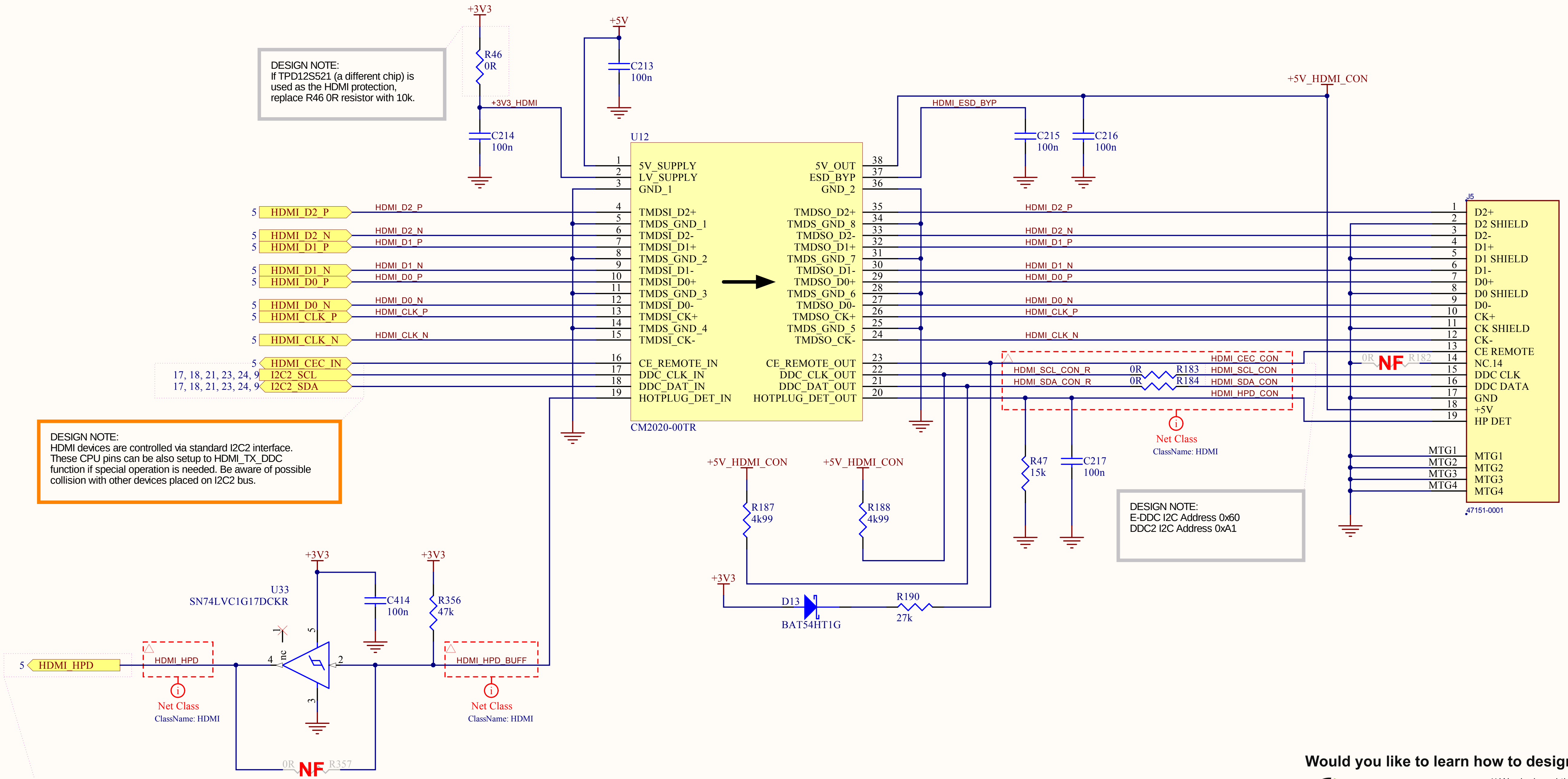
HDMI Connector



+3V3
R46
0R
+3V3_HDMI
C214
100n
+5V
C213
100n
U12
CM2020-00TR
5V_SUPPLY
LV_SUPPLY
GND_1
TMDSI_D2+
TMDS_GND_1
TMDSI_D2-
TMDSI_D1+
TMDS_GND_2
TMDSI_D1-
TMDSI_D0+
TMDS_GND_3
TMDSI_D0-
TMDSI_CK+
TMDS_GND_4
TMDSI_CK-
CE_REMOTE_IN
DDC_CLK_IN
DDC_DAT_IN
HOTPLUG_DET_IN
5V_OUT
ESD_BYP
GND_2
TMDSO_D2+
TMDS_GND_8
TMDSO_D2-
TMDSO_D1+
TMDS_GND_7
TMDSO_D1-
TMDSO_D0+
TMDS_GND_6
TMDSO_D0-
TMDSO_CK+
TMDS_GND_5
TMDSO_CK-
CE_REMOTE_OUT
DDC_CLK_OUT
DDC_DAT_OUT
HOTPLUG_DET_OUT
HDMI_ESD_BYP
C215
100n
C216
100n
+5V_HDMI_CON
5 HDMI_D2_P
5 HDMI_D2_N
5 HDMI_D1_P
5 HDMI_D1_N
5 HDMI_D0_P
5 HDMI_D0_N
5 HDMI_CLK_P
5 HDMI_CLK_N
5 HDMI_CEC_IN
17, 18, 21, 23, 24, 9 I2C2_SCL
17, 18, 21, 23, 24, 9 I2C2_SDA
HDMI_CEC_CON
HDMI_SCL_CON_R
HDMI_SDA_CON_R
HDMI_SCL_CON
HDMI_SDA_CON
HDMI_HPD_CON
0R R183
0R R184
0R NF R182
Net Class
ClassName: HDMI
J5
47151-0001
D2+
D2 SHIELD
D2-
D1+
D1 SHIELD
D1-
D0+
D0 SHIELD
D0-
CK+
CK SHIELD
CK-
CE REMOTE
NC.14
DDC CLK
DDC DATA
GND
+5V
HP DET
MTG1
MTG2
MTG3
MTG4
R47
15k
C217
100n
+5V_HDMI_CON
R187
4k99
R188
4k99
+3V3
D13
BAT54HT1G
R190
27k
U33
SN74LVC1G17DCKR
C414
100n
R356
47k
5 HDMI_HPD
HDMI_HPD
HDMI_HPD_BUFF
0R NF R357

DESIGN NOTE:
If TPD12S521 (a different chip) is used as the HDMI protection, replace R46 0R resistor with 10k.

DESIGN NOTE:
HDMI devices are controlled via standard I2C2 interface. These CPU pins can be also setup to HDMI_TX_DDC function if special operation is needed. Be aware of possible collision with other devices placed on I2C2 bus.

DESIGN NOTE:
E-DDC I2C Address 0x60
DDC2 I2C Address 0xA1

DESIGN NOTE:
From CM2020 datasheet, the HOTPLUG_DET_IN pin specification is not clear. A schmitt buffer is added and after testing can be bypassed by R357.

Title: OpenRex		Variant: Production	
Page Contents: [16] - HDMI.SchDoc		Checked by	
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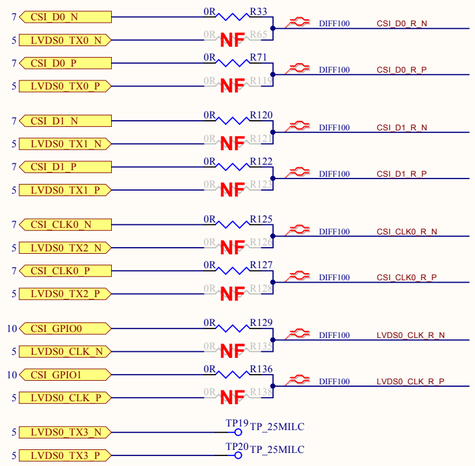
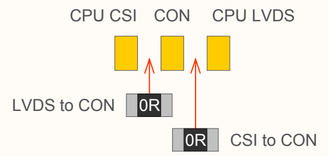
LVDS / CSI, LCD / CSI1 CONNECTORS, TOUSCHSCREEN

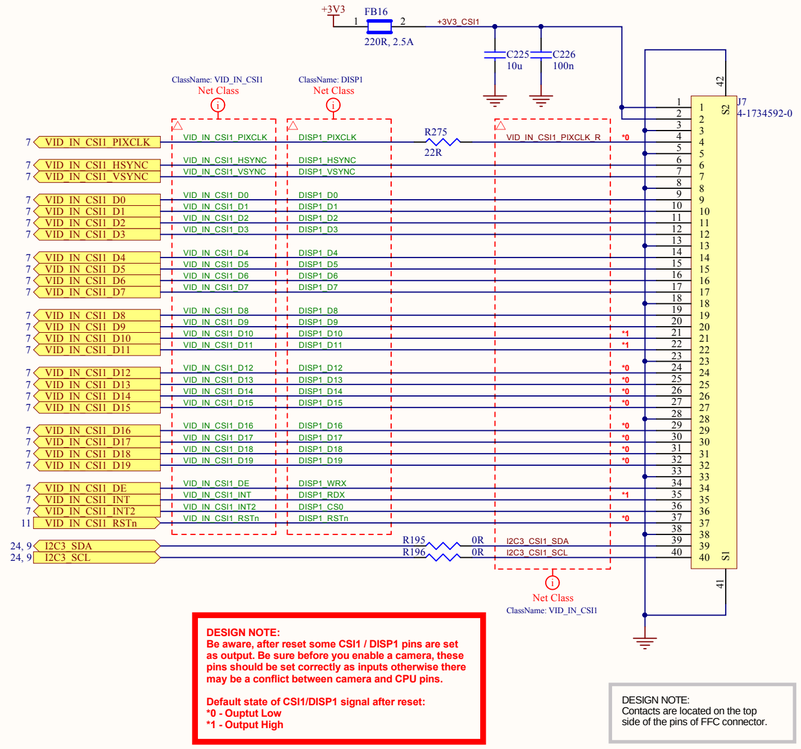
CSI / LVDS Routing



DESIGN NOTE:
Fit only one resistor per one signal according to the picture below.



CSI1 / DISP1 Connector



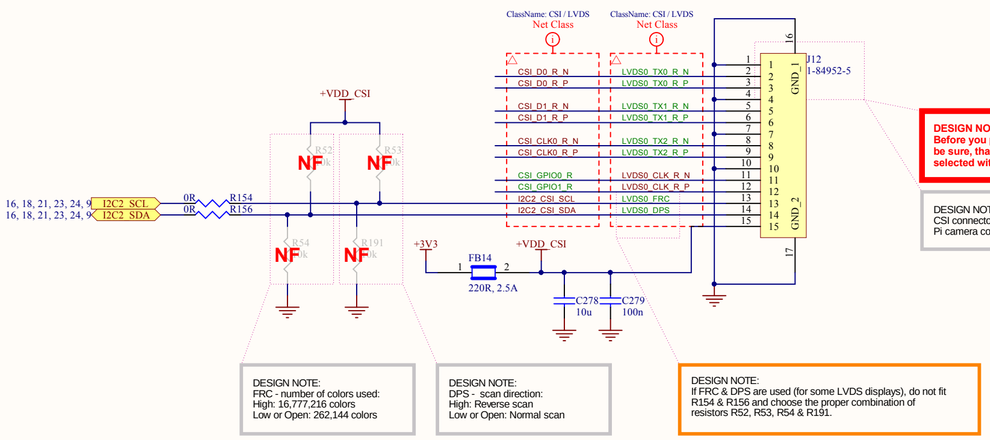
DESIGN NOTE:
Be aware, after reset some CSI1 / DISP1 pins are set as output. Be sure before you enable a camera, these pins should be set correctly as inputs otherwise there may be a conflict between camera and CPU pins.

Default state of CSI1/DISP1 signal after reset:
***0 - Ouptut Low**
***1 - Output High**

DESIGN NOTE:
Contacts are located on the top side of the pins of FFC connector.

CSI Camera / LVDS Connector

(Raspberry Pi compatible)



DESIGN NOTE:
Before you plug in cable into connector J12, be sure, that the correct interface is selected with the optional series resistors.

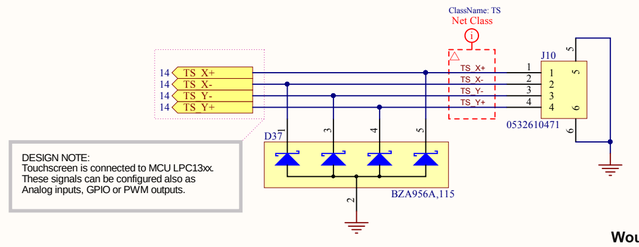
DESIGN NOTE:
CSI connector is pin compatable with Raspbery Pi camera connector.

DESIGN NOTE:
FRC - number of colors used:
High: 16,777,216 colors
Low or Open: 262,144 colors

DESIGN NOTE:
DPS - scan direction:
High: Reverse scan
Low or Open: Normal scan

DESIGN NOTE:
If FRC & DPS are used (for some LVDS displays), do not fit R154 & R156 and choose the proper combination of resistors R52, R53, R54 & R191.

Touchscreen Connector



DESIGN NOTE:
Touchscreen is connected to MCU LPC13xx. These signals can be configured also as Analog inputs, GPIO or PWM outputs.

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Title:	OpenRex	Variant:	Production
Page Contents:	[17] - LVDS, CSI, LCD, TSC.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
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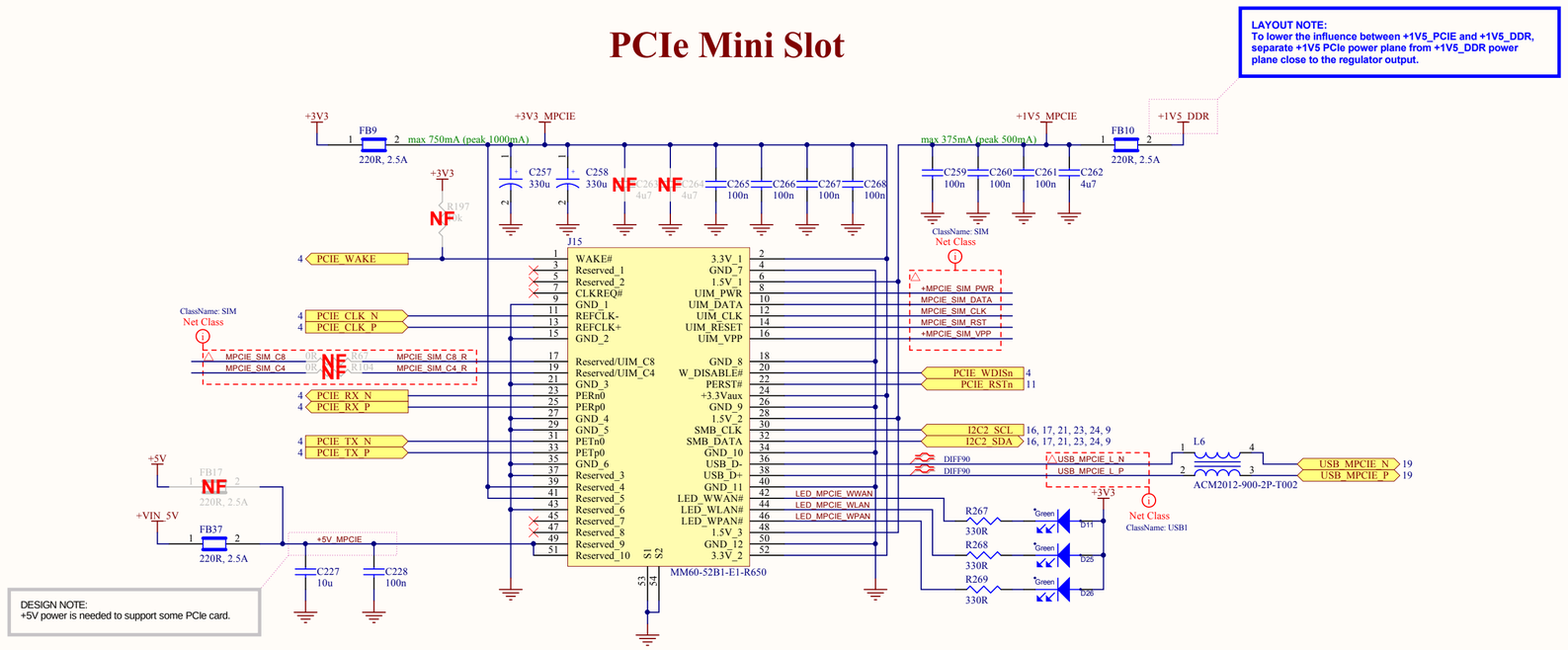
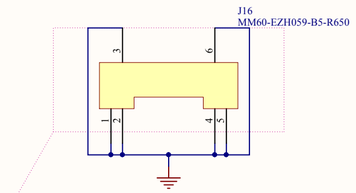
PCIE MINI

PCIe Mini Slot

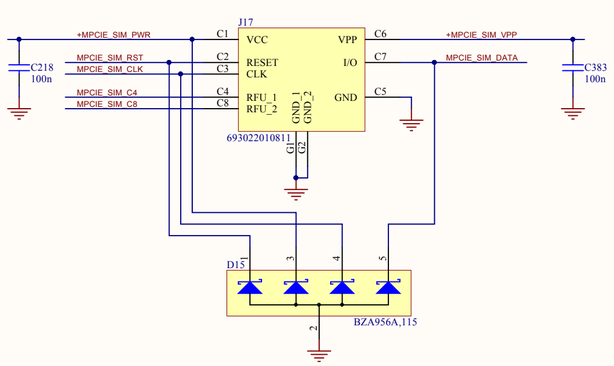


Card Latch for PCIe Mini Card

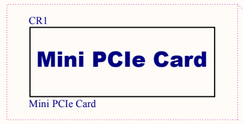


LAYOUT NOTE:
Distance between PCIe Mini connector and latch (hole to hole - the bigger ones):
X = 50.3mm
Y = 0.4mm
See also
https://jae-connectors.com/en/pdf_download_exec.cfm?param=SJ105219.pdf

SIM card for PCIe Mini



3D Model of PCIe Mini Card



LAYOUT NOTE:
This is a stand off slot. The maximum allowed component height in the PCIe Mini Card area is 2.2mm.

3D Model of Micro SIM Card

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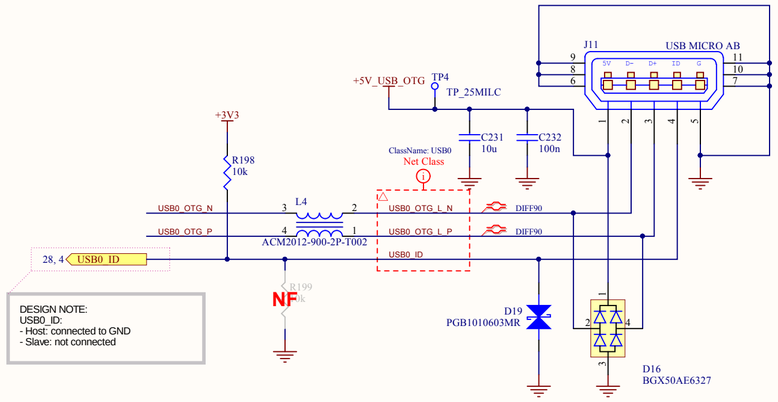
Page Contents:	[18] - PCIE MINI.SchDoc		Checked by
Size:	DWG NO		Revision: V111
Date: 10. 1. 2016	Designed by www.fedevel.com	Sheet 18 of	31

USB

USB0 OTG Connector

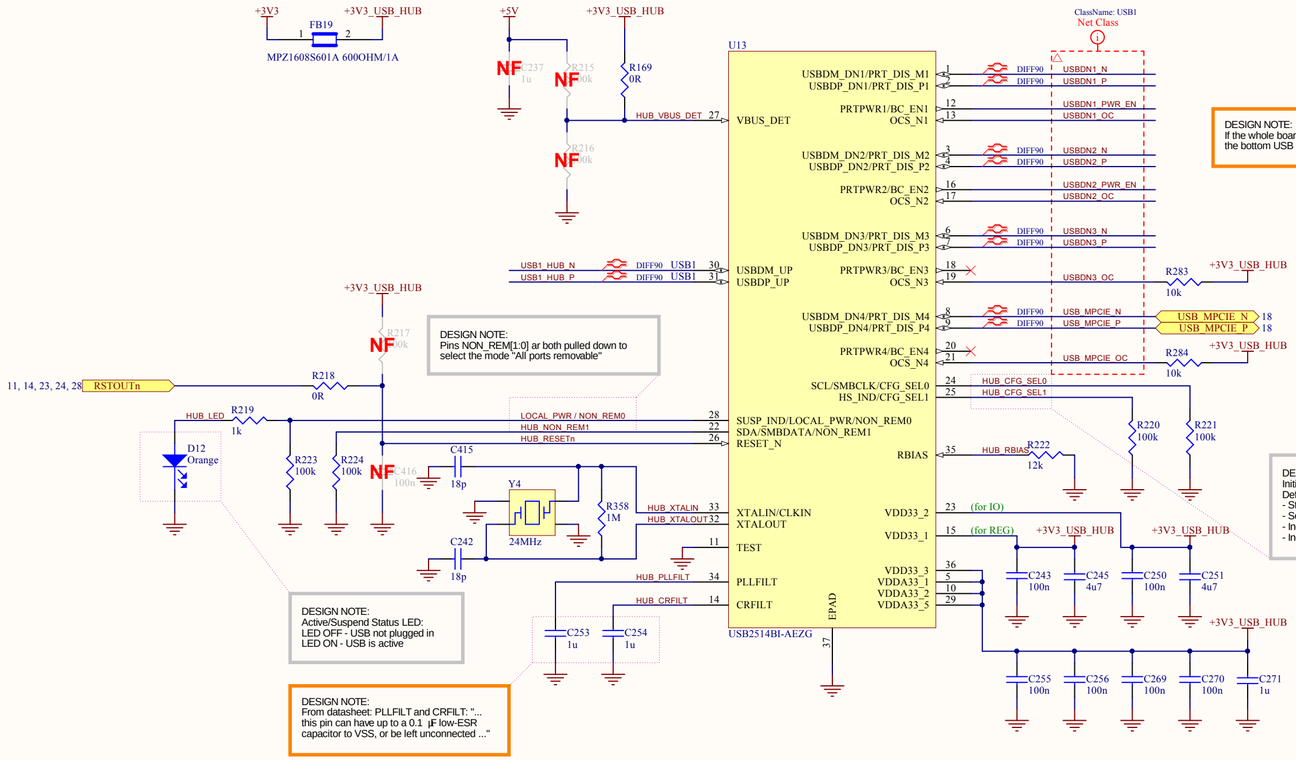


DESIGN NOTE:
The maximum current through USB Micro Connector is 1.8A per contact.

DESIGN NOTE:
To power OpenRex board from Micro USB connector, the power jack must not be inserted.

DESIGN NOTE:
USB0_ID:
- Host: connected to GND
- Slave: not connected

USB1 Hub



DESIGN NOTE:
Pins NON_REM[1:0] ar both pulled down to select the mode "All ports removable"

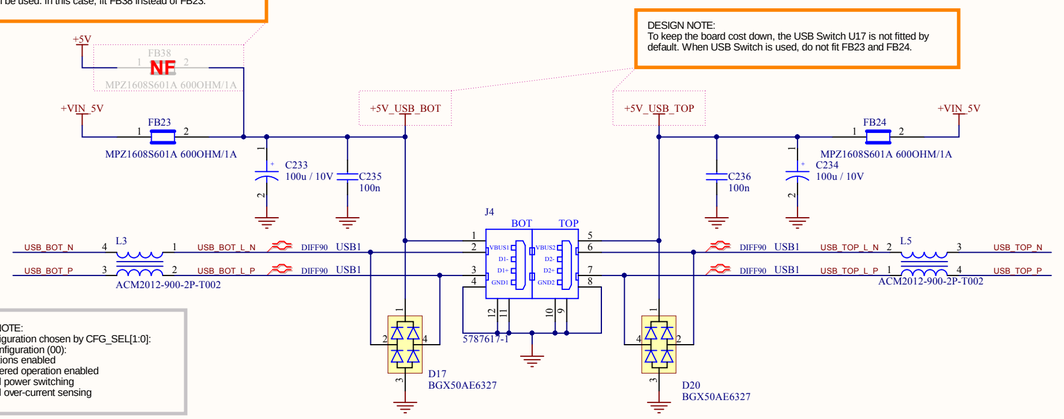
DESIGN NOTE:
Active/Suspend Status LED:
LED OFF - USB not plugged in
LED ON - USB is active

DESIGN NOTE:
From datasheet: PLLFILT and CRFILT: "... this pin can have up to a 0.1 µF low-ESR capacitor to VSS, or be left unconnected ..."

DESIGN NOTE:
If the whole board is powered from a battery (input voltage is lower than +5V), the bottom USB still can be used. In this case, fit FB38 instead of FB23.

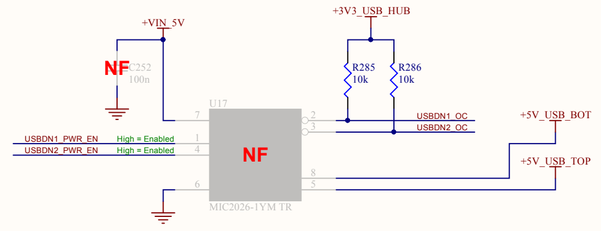
DESIGN NOTE:
Initial configuration chosen by CFG_SEL[1:0]:
Default configuration (00):
- Strap options enabled
- Self-powered operation enabled
- Individual power switching
- Individual over-current sensing

Stacked USB-A Connector



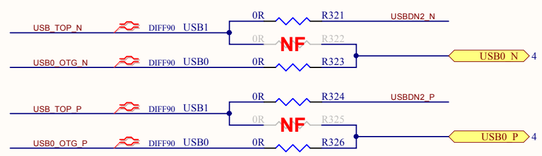
DESIGN NOTE:
To keep the board cost down, the USB Switch U17 is not fitted by default. When USB Switch is used, do not fit FB23 and FB24.

USB Switch

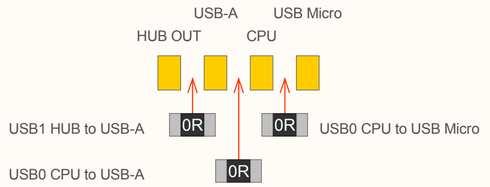


USB Routing Options

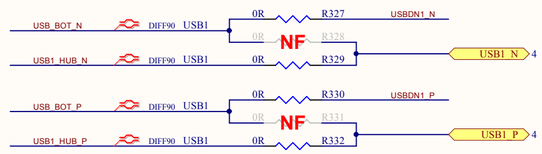
USB0 Routing



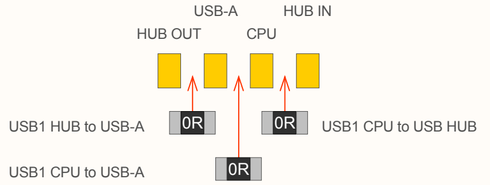
DESIGN NOTE:
Use one of the options to fit series resistors according to the picture below.



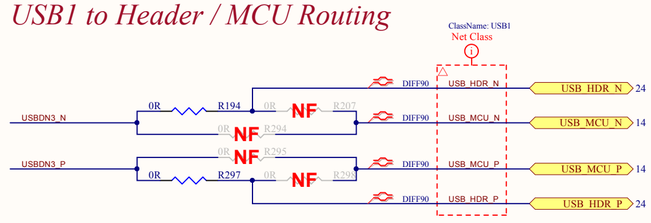
USB1 Routing



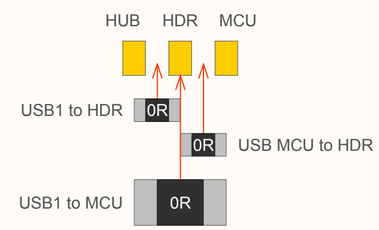
DESIGN NOTE:
Use one of the options to fit series resistors according to the picture below.



USB1 to Header / MCU Routing



DESIGN NOTE:
This configuration is available only when USB Hub is used.
Fit only one resistor per signal according to the picture below.



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Title:	OpenRex	Variant:	Production
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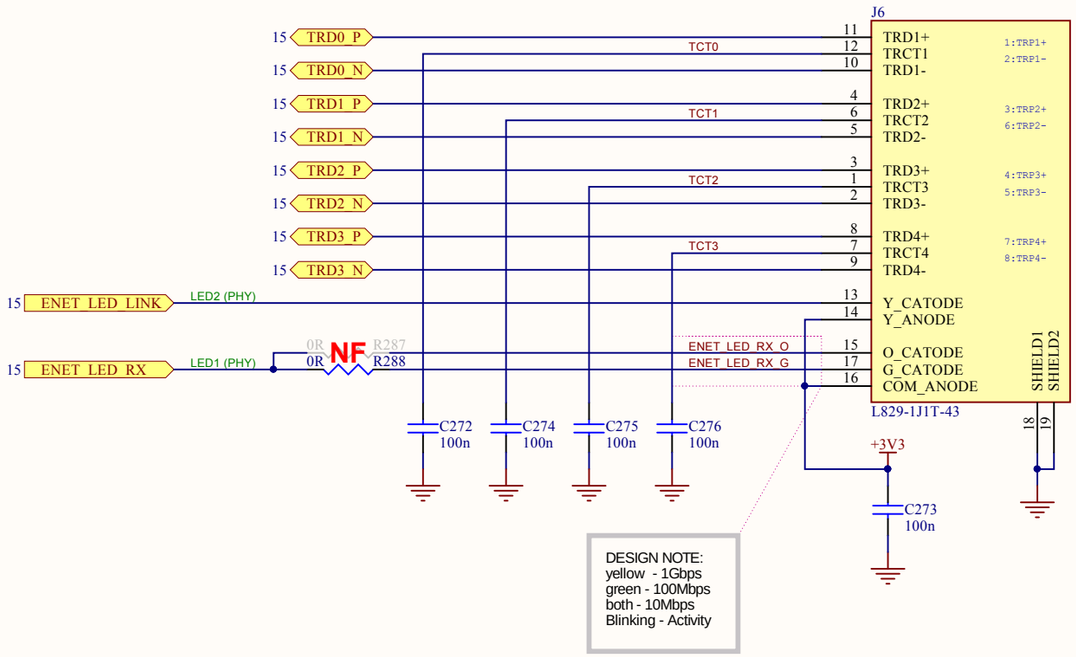
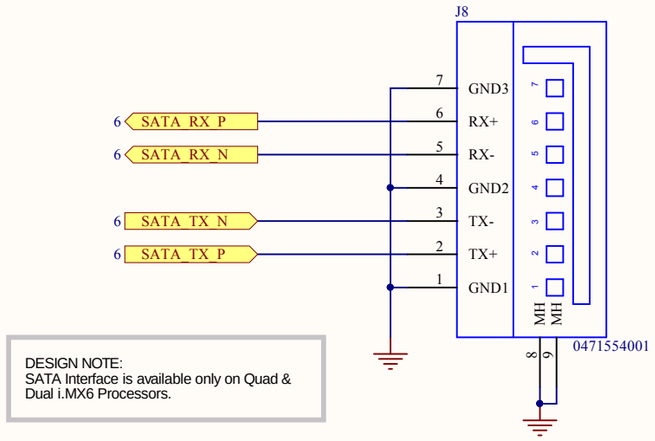
ETHERNET, SATA

RJ45 + Magnetics



SATA



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AUDIO

DESIGN NOTE:
External VDDD supply is required.

+1V5_DDR — FB20 NF MPZ1608S601A 600OHM/1A — +VDDD

+1V8_AUDIO — FB11 MPZ1608S601A 600OHM/1A — +VDDD

+1V8_AUDIO — FB26 NF MPZ1608S601A 600OHM/1A

+3V3 — FB12 MPZ1608S601A 600OHM/1A — +VDDIO

+3V3 — FB13 MPZ1608S601A 600OHM/1A — +VDDA

C280 10u, C281 100n (+VDDIO), C282 100n (+VDDD), C283 100n (+VDDA)

U14 SGTL5000XNAA3R2

TP7 TP_25MILC	MIC_LINEIN_L 14	LINEIN_L	
TP41 TP_25MILC	MIC_LINEIN_R 13	LINEIN_R	
	MIC_IN 15	MIC	
	MIC_BIAS 16	MIC_BIAS	
16, 17, 18, 23, 24, 9 I2C2_SDA	27	CTRL_DATA	
16, 17, 18, 23, 24, 9 I2C2_SCL	29	CTRL_CLK	
9 AUD3_RXD	25	I2S_DOUT	
9 AUD3_TXD	26	I2S_DIN	
9 AUD3_TXFS	23	I2S_LRCLK	
9 AUD3_TXC	24	I2S_SCLK	
9 AUD3_CLK	21	SYS_MCLK	
	31	CTRL_ADR0_CS	
	32	CTRL_MODE	
		LINEOUT_L	12
		LINEOUT_R	11
		HP_L	6 AUD_HP_L
		HP_R	2 AUD_HP_R
		HP_VGND	4 AUD_HP_VGND
		VAG	10 AUD_VAG
		CPFILT	18
		NC_1	8
		NC_2	9
		NC_3	17
		NC_4	19
		NC_5	22
		NC_6	28
		AGND	7
		GND_1	1
		GND_2	3
		EPAD	33

I2C ADDRESS = 0x14/0x15

220u, 4V 1 — C290 — HP_OUT_L

220u, 4V 1 — C291 — HP_OUT_R

C292 100n NF — R234 0R

DESIGN NOTE:
If either VDDIO or VDDA is above 3V, the CPFILT pin must not be connected to capacitor.

DESIGN NOTE:
Source for the audio filters is http://www.cirrus.com/en/pubs/rdDatasheet/CDB4207_DB1.pdf

Headphones

HP_OUT_R — BLM15AX601SN1D FB21 — FIL_HP_OUTR

HP_OUT_L — BLM15AX601SN1D FB22 — FIL_HP_OUTL

C284 100n, R232 33R, C288 100pF, R230 15k

C285 100n, R233 33R, C289 100pF, R231 15k

C286 270pF, C287 270pF

Mic In

MIC_BIAS — R235 2k2, C293 1u

MIC_IN — 100n C294 — MIC_IN_C — BLM15AX601SN1D FB18 — FIL_MIC_IN

C295 270pF

Headphones & Mic Jack

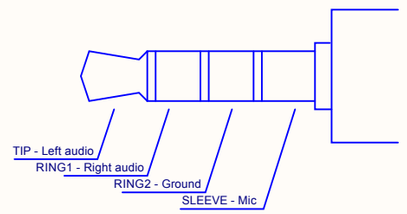
DESIGN NOTE:
Audio jack is designed to support CTIA / AHJ standard.

J14 FC68125

6	SL&RING 6
2	RING 2
4	TIP_2 4
3	TIP_1 3
1	SLEEVE 1
5	HOLE_1
7	HOLE_2

DESIGN NOTE:
Alternate audio jack connector: MJ-2135
http://uk.farnell.com/pro-signal/mj-2135/connector-rca-jack-3-5mm-tht-4way/dp/1267377

3.5mm 4-pole jack reference
(TRSS standard - CTIA / AHJ)



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Title: OpenRex		Variant: Production	
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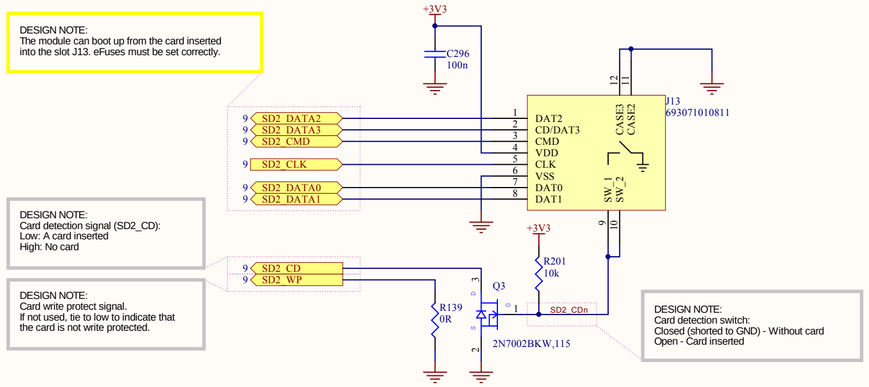
SD CARD, FLASH, EEPROM

Micro SD Slot

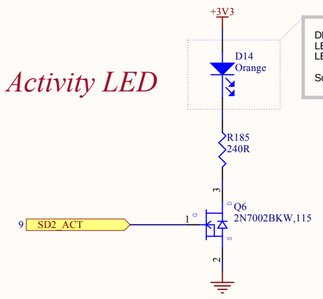


3D Model of Micro SD2 Card

Firmware

DESIGN NOTE:
To download firmware go to : http://www.imx6rex.com/

uSD2 Activity LED



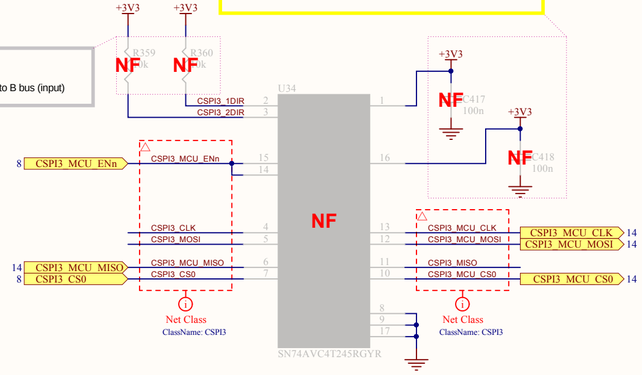
DESIGN NOTE:
LED on (SD2_ACT High): SD interface busy
LED off (SD2_ACT Low): SD interface in idle

Software support is required.

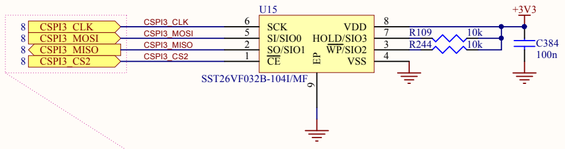
SPI Switch

DESIGN NOTE:
Be aware: the SPI signals from CPU are connected to both ports, A & B. For that reason, the VccA and VccB pins must be connected to the same voltage.

DESIGN NOTE:
Direction:
A data (output) goes to B bus (input)

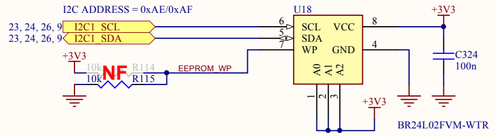


SPI NOR FLASH



DESIGN NOTE:
SPI Flash is the prefered device to boot from. SPI interface is not affected by possible SD card boot errata ERR006282.

EEPROM



SPI Switch Bypass

DESIGN NOTE:
SN74AVC4T245 can be used if signal integrity needs to be improved. In that case, do not fit bypass resistors R361-R364.

DESIGN NOTE:
If SN74AVC4T245 is used, the MCU can operate as a slave only.

SPI3 Testpoints

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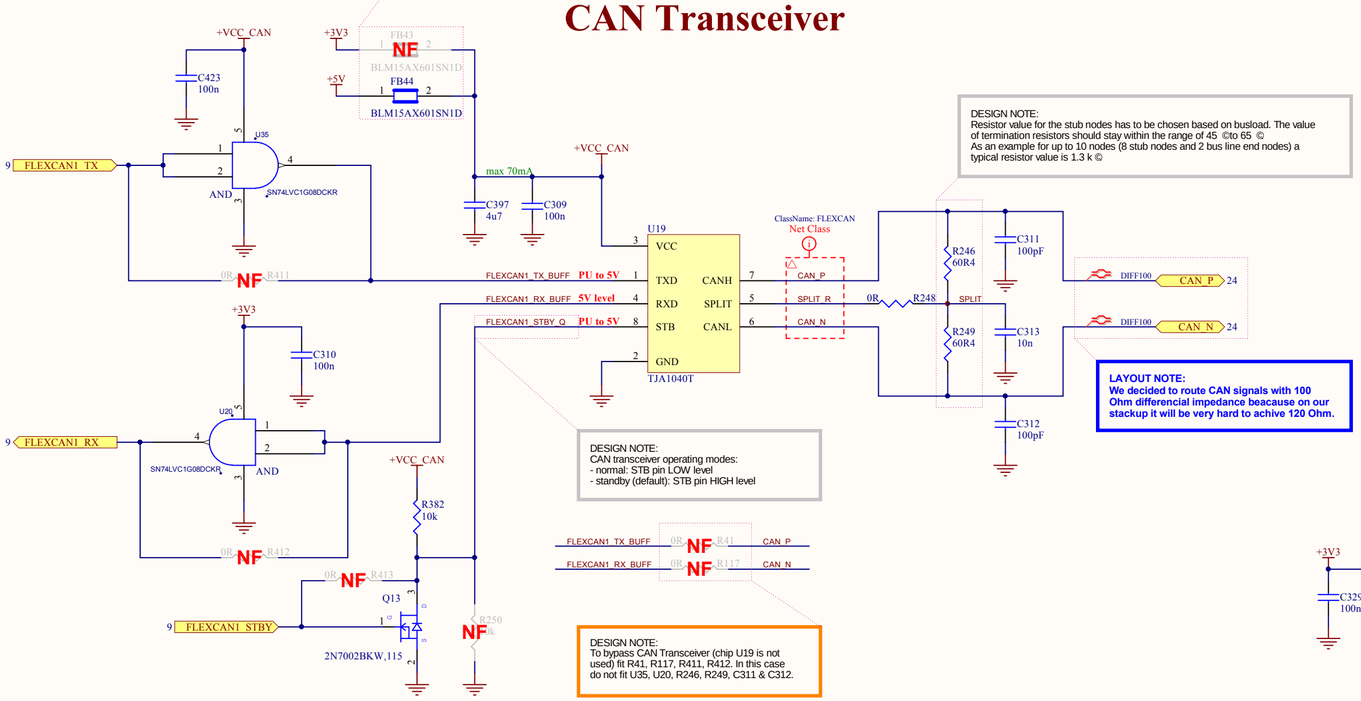
SENSORS, IR, CAN

DESIGN NOTE:
An alternate +3V3 level CAN transceiver SN65HVD230DR can be used.

In that case, the buffers are not needed. Fit R411, R412, R413 instead.
Do not forget to change the supply voltage (fit FB43 and do not fit FB44).

CAN Transceiver



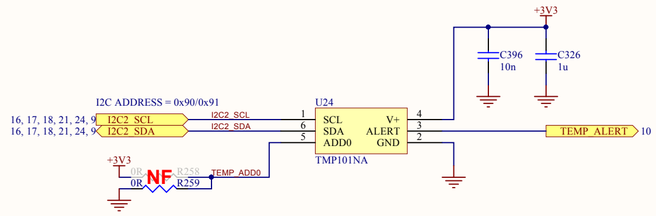
DESIGN NOTE:
Resistor value for the stub nodes has to be chosen based on busload. The value of termination resistors should stay within the range of 45 © to 65 ©
As an example for up to 10 nodes (8 stub nodes and 2 bus line end nodes) a typical resistor value is 1.3 k ©

DESIGN NOTE:
CAN transceiver operating modes:
- normal: STB pin LOW level
- standby (default): STB pin HIGH level

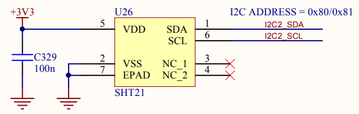
LAYOUT NOTE:
We decided to route CAN signals with 100 Ohm differencial impedance beacause on our stackup it will be very hard to achive 120 Ohm.

DESIGN NOTE:
To bypass CAN Transceiver (chip U19 is not used) fit R41, R117, R411, R412. In this case do not fit U35, U20, R246, R249, C311 & C312.

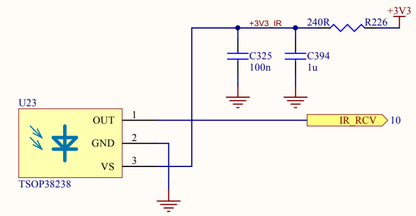
Temperature sensor



Humidity sensor



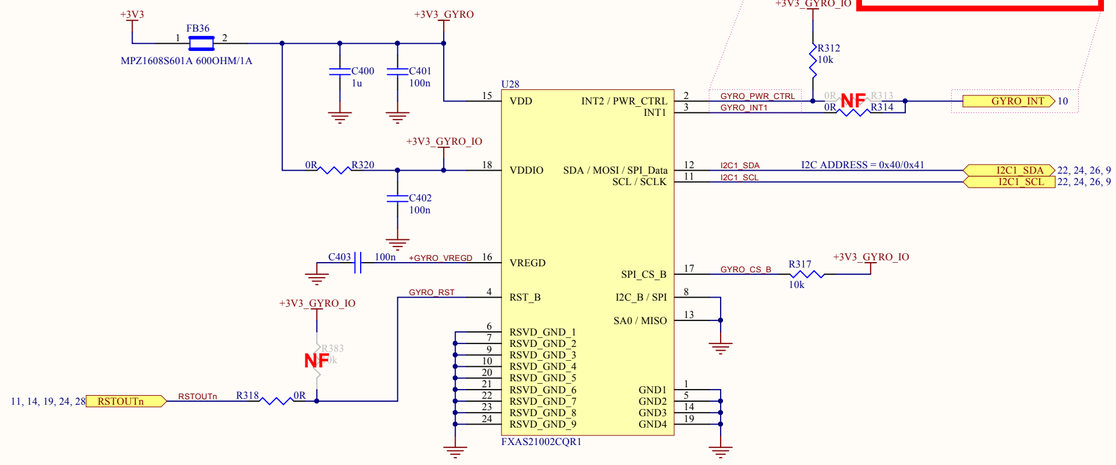
IR Receiver



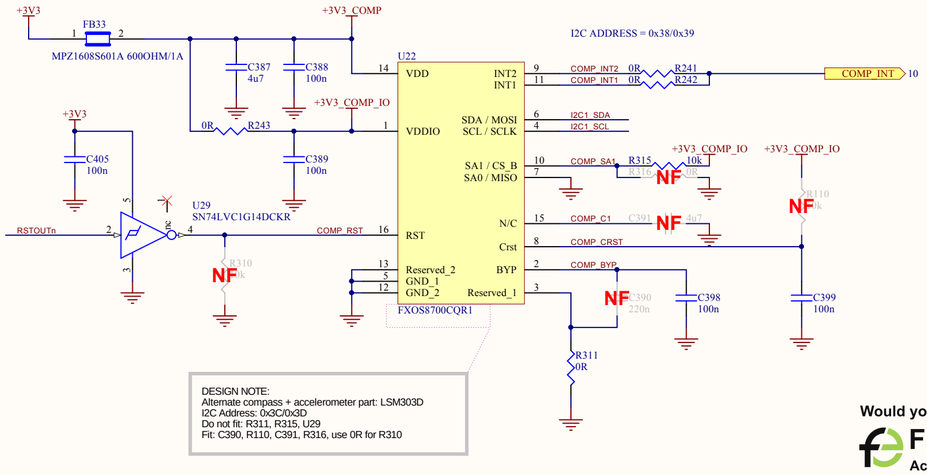
Gyroscope

AftDESIGN NOTE:
After reset, the Gyroscope is in Standby (bits ACTIVE and READY in CTRL_REG1 are low) and pin INT2 / PWR_CTRL is setup as an interrupt.

DESIGN NOTE:
Be aware: After reset, the INT1 and INT2 / PWR_CTRL are setup as push-pull outputs!



Compass + Accelerometer



DESIGN NOTE:
Alternate compass + accelerometer part: LSM303D
I2C Address: 0x3C/0x3D
Do not fit: R311, R315, U29
Fit: C390, R110, C391, R316, use 0R for R310

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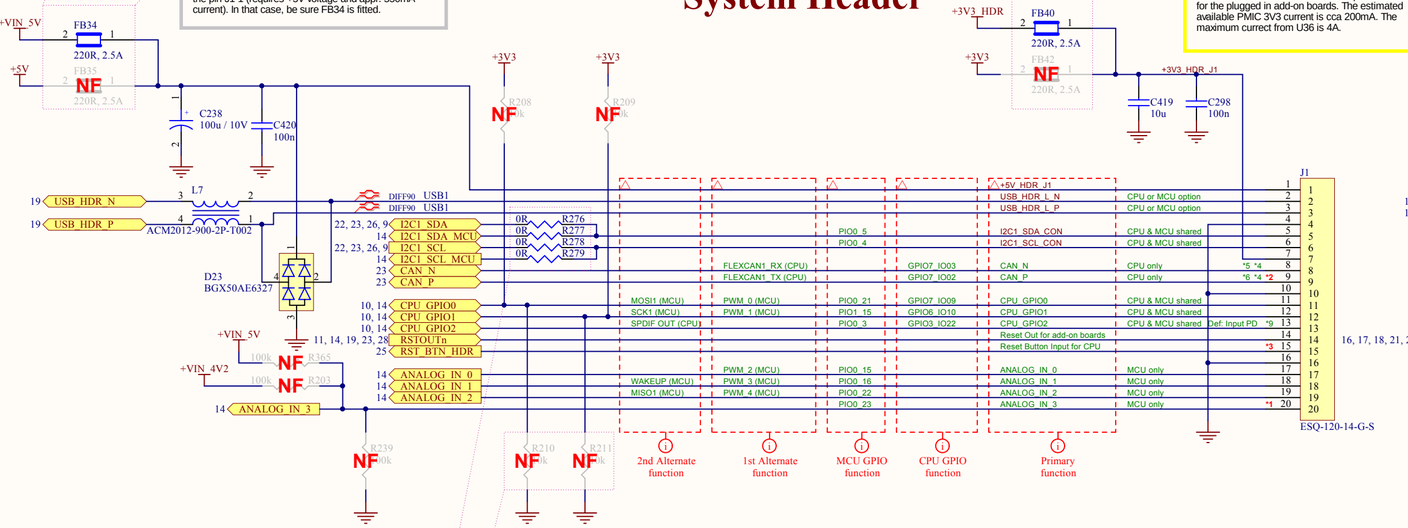
HEADERS, UART

DESIGN NOTE:
Fit FB35 (and do not fit FB34) when battery is supplying the board. Check the maximum current for +5V first.

DESIGN NOTE:
A 2.5" SATA hard drive can be powered up through the pin J1-1 (requires +5V voltage and appr. 550mA current). In that case, be sure FB34 is fitted.

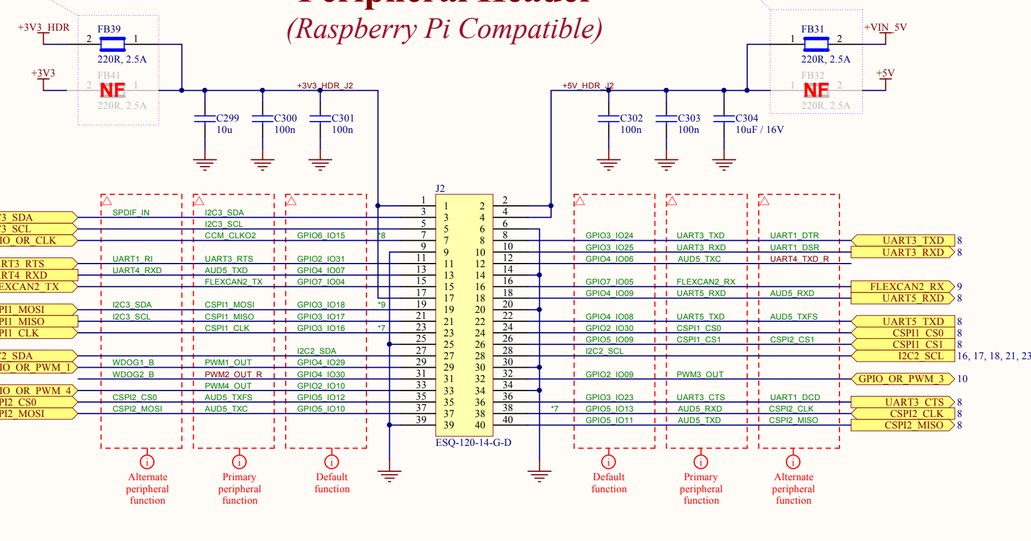
System Header

DESIGN NOTE:
To save some board cost, the strong 3V3 U36 power supply can be left unfitted. In that case, be sure that PMIC can deliver all the required current for the plugged in add-on boards. The estimated available PMIC 3V3 current is cca 200mA. The maximum currect from U36 is 4A.



Peripheral Header
(Raspberry Pi Compatible)

DESIGN NOTE:
Fit FB32 (and do not fit FB31) when battery is supplying the board. Check the maximum current for +5V first.



DESIGN NOTE:
I2C1 bus bypass options:
R276 - R279 fitted, R277 & R279 fitted (default) - system I2C connected to the J1 header and MCU
R276 & R278 fitted; R277 & R279 not fitted - system I2C connected to the J1 header, MCU is disconnected from I2C
R276 & R278 not fitted; R277 & R279 fitted - system I2C disconnected; MCU I2C or GPIO function on the J1 header. if MCU I2C is used, fit also R290 & R291 pullups.

DESIGN NOTE:
Incorrect implementation of resistors R208 - R211 can setup undefined value on CPU_CPIO0 & 1. Be sure, you disable internal pullups for MCU first. Also, be aware, that the CPU_GPIO2 pin has an internal pull down resistor enabled by default.

DESIGN NOTE:
All signals on connectors J1 & J2 are pulled high by default (unless noted otherwise). Default states may be different comparing to the Raspberry Pi pull up/down default configuration.

DESIGN NOTE:
All signals on J1 and J2 connector are 3V3 level compatible (unless otherwise noted). Connecting higher voltage may damage the board.

Exceptions:
***1 This pin my be connected to input voltage (when R239, R203 or R365 is fitted) to support input voltage monitoring**
***2 Ouput of this signal can be as high as +5V**
***3 Be careful: This pin may be connected to +3V0_SVNVS**

DESIGN NOTE:
*4 Pins CANH & CANL can be used as standard GPIOs or FLEXCAN pins. Before using these functions, be sure that the CAN Transceiver is not fitted (U19, U2o, U35, R246, R249, C311 & C312 NF) and signals are bypassed (R41, R117, R411, R412 fitted).

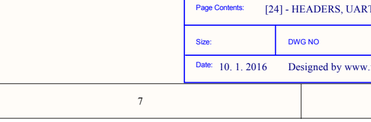
DESIGN NOTE:
*5 When CANL signal is bypassed and buffer U20 is fitted, this pin can be used as a 5V tolerant input.

*6 When CANH signal is bypassed and buffer U35 is fitted, this pin can be used as a 5V CPU output.

DESIGN NOTE:
*7 These signals have series 22R resistor in signal path.

*8 If I2S Audio (AUD5) is used throught the J2 header, GPIO_OR_CLK can be used as the master clock.

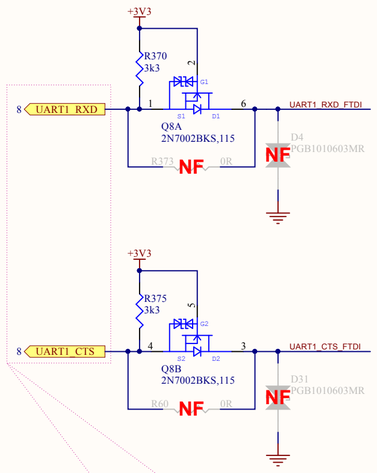
DESIGN NOTE:
*9 These signals can be used as an optional SPDIF digital audio interface:
- SPDIF_OUT: use CPU_GPIO2
- SPDIF_IN: use I2C3_SDA. In this case, do not place any other devices on the I2C3 bus.



DESIGN NOTE:
If some add-on boards (compatible with short Raspberry Pi connector) require PWM Signal connected to J2-pin12, these signals can be swapped using resistors R366-R369.

UART 1 - Debug console (+3V3)

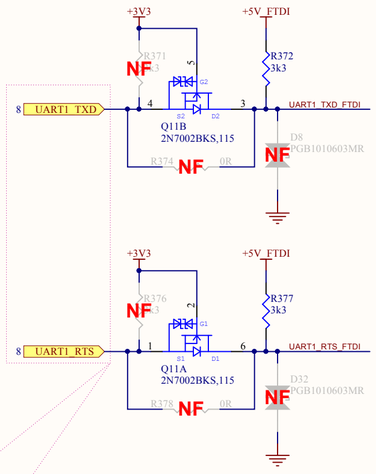
Buffers for CPU Input Pins



DESIGN NOTE:
Buffers for UART1 are designed to isolate the CPU when the board is turned off and FTDI cable is still connected. Without the isolation, leaking currect from the plugged FTDI cable can prevent CPU from booting.

DESIGN NOTE:
If isolation is not required, buffers can by bypassed through R60, R373, R374 and R378 resistors.

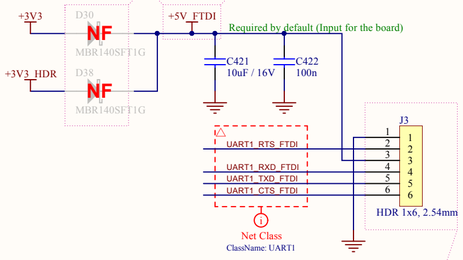
Buffers for CPU Output Pins



Serial console header

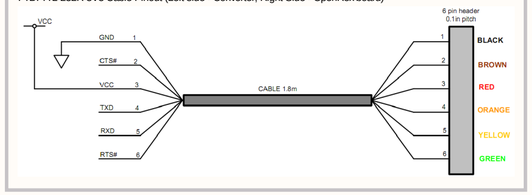
DESIGN NOTE:
In the case, when J3 is not used for debugging, but as a standard UART interface,+3V3 power can be provided on J3 pin 3 through D30 or D38.

DESIGN NOTE:
If isolation circuits are fitted, the UART signals on J3 support signal levelling defined by device connected to the J3 and voltage connected to J3 pin 3 (e.g. 3V3, 5V, ...)



DESIGN NOTE:
Serial console header is designed to be used with FTDI TTL-232R-3V3 TTL to USB Serial Converter Cable by default:
http://www.ftdichip.com/Support/Documents/DataSheets/Cables/DS_TTL-232R_CABLES.pdf

DESIGN NOTE:
FTDI TTL-232R-3V3 Cable Pinout (Left side - Converter; Right Side - OpenRex board)



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LEDS, BUTTONS

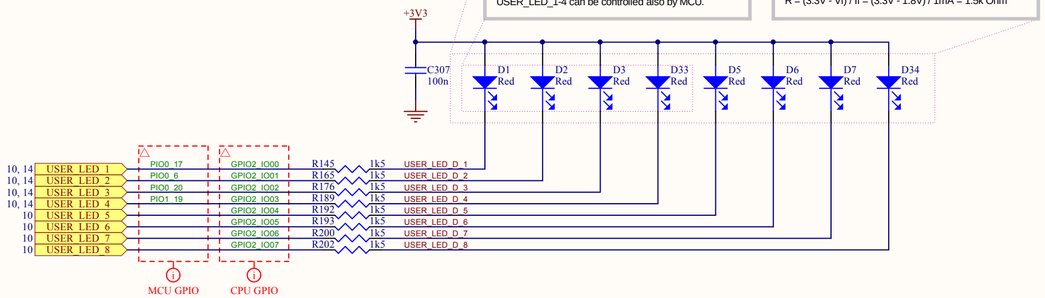
User LEDS

DESIGN NOTE:
When driving LEDs, do not set the pins as outputs. Set them as an open drain and use internal pullup to prevent conflict with MCU pins. Do the same for MCU.

DESIGN NOTE:
i.MX6 datashet does not show the maximum CPU output pin current. Only what is guaranteed, is a 1mA testing current mentioned in Table 22 (datasheet IMX6DQCEC.pdf).

DESIGN NOTE:
USER_LED_1-4 can be controlled also by MCU.

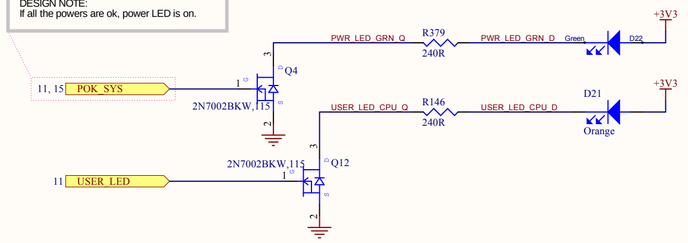
DESIGN NOTE:
Series resistor calculation (for forward current 1mA)
R = (3.3V - Vf) / If = (3.3V - 1.8V) / 1mA = 1.5k Ohm



LEDs

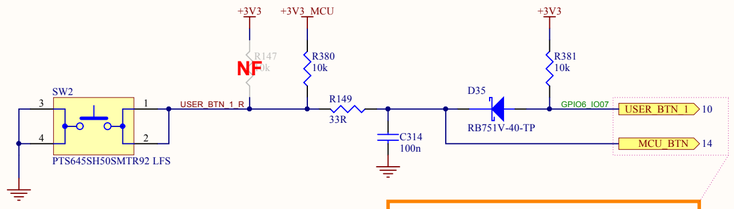
Power, CPU User LEDs

DESIGN NOTE:
If all the powers are ok, power LED is on.



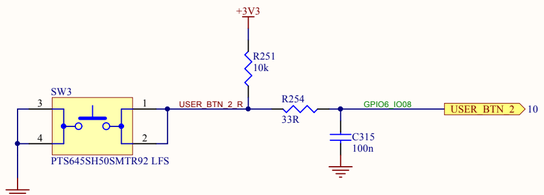
User / Android Buttons

Home / Wake Up Button

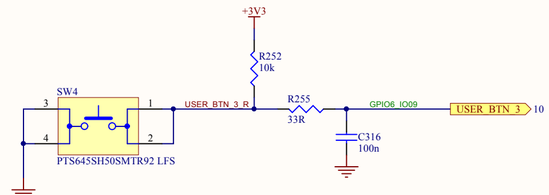


DESIGN NOTE:
Home / Wake up button can be used by both: CPU and MCU.

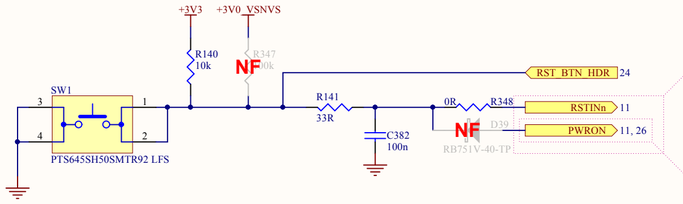
Back / Volume- Button



Recent / Volume+ Button



Reset / Power Button



DESIGN NOTE:
Reset / Power On-Off Button function:
- RSTINn - the button resets the CPU and peripherals (default) - Fit R140 & R348, do not fit R347 & D39
- PWRON - the button is connected to PMIC and resets or turnes on / off the whole board - Fit R347 & D39, do not fit R140 & R348

DESIGN NOTE:
PMIC PWRON button function (based on PWRON_CFG setting in PMIC registers)
- PWRON_CFG = Low (level sensitive): reset all the sources when button pressed
- PWRON_CFG = High (edge sensitive): button acts as a power signal for the board
  - button pressed momentarily - board turns on
  - button pressed for more than 4 seconds - boards tuns off or put to sleep mode

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POWER PMIC

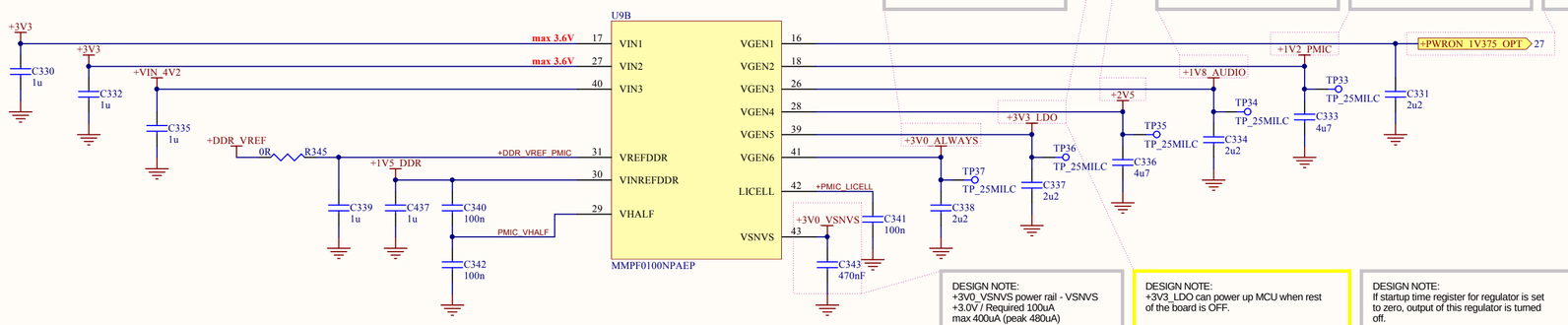
PMIC LDO Outputs

Firmware

FIRMWARE_FOR_U9

FIRMWARE PMIC

OpenRex PMIC 1.0



DESIGN NOTE:
+3V3_LDO power rail - VGEN5
+3.3V / Required 0.1A
max 0.1A (peak 0.12A)

DESIGN NOTE:
+2V5 power rail - VGEN4
+2.5V / Required 0.35A
max 0.35A (peak 0.42A)

DESIGN NOTE:
+3V0_ALWAYS power rail - VGEN6
+3.0V / Required 0.15A
max 0.2A (peak 0.22A)

DESIGN NOTE:
+1V8_AUDIO power rail - VGEN3
+1.8V / Required 0.03A
max 0.1A (peak 0.12A)

DESIGN NOTE:
+1V2_ETH power rail - VGEN2
+1.2V / Required 0.25A
max 0.25A (peak 0.29A)

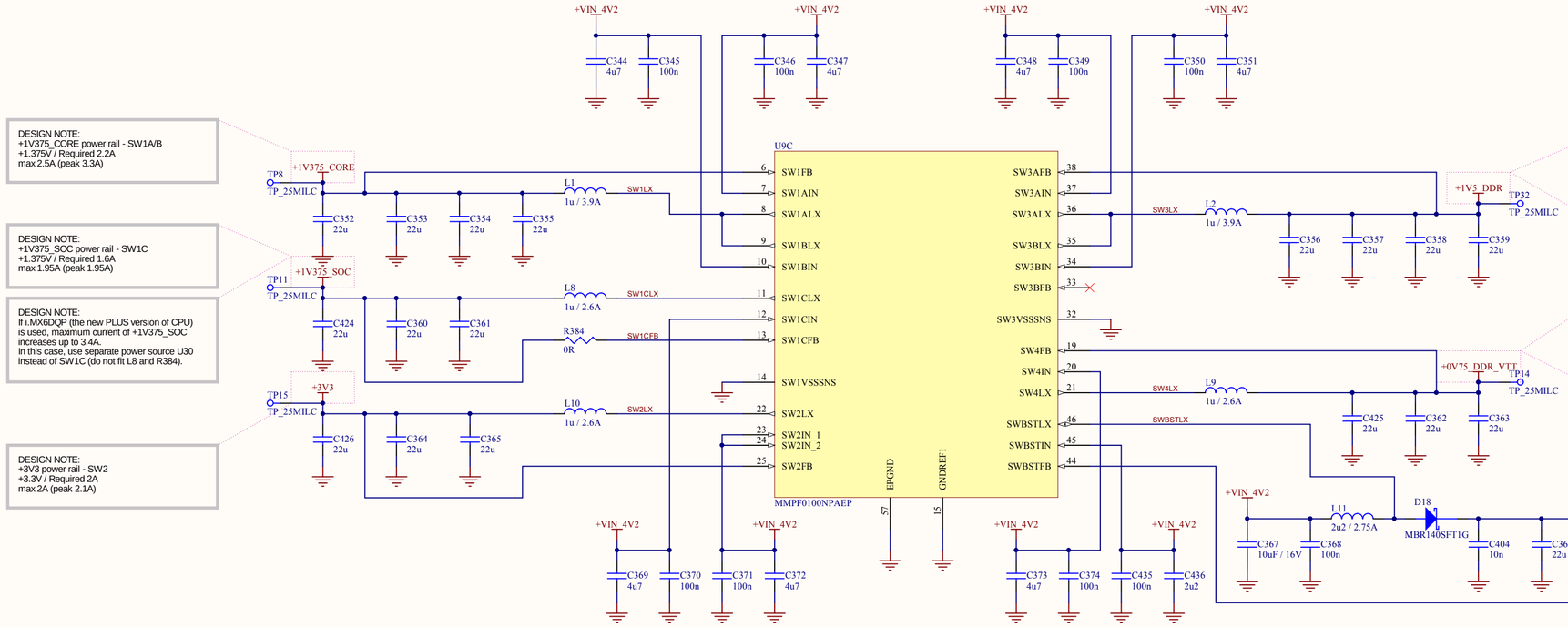
DESIGN NOTE:
Power rail VGEN1 is used as a Power Enable signal for optional high current +1V375_SOC source.

DESIGN NOTE:
+3V0_VSNVS power rail - VSNVS
+3.0V / Required 100uA
max 400uA (peak 480uA)

DESIGN NOTE:
+3V3_LDO can power up MCU when rest of the board is OFF.

DESIGN NOTE:
If startup time register for regulator is set to zero, output of this regulator is turned off.

PMIC Switched Outputs



DESIGN NOTE:
+1V375_CORE power rail - SW1A/B
+1.375V / Required 2.2A
max 2.5A (peak 3.3A)

DESIGN NOTE:
+1V375_SOC power rail - SW1C
+1.375V / Required 1.6A
max 1.95A (peak 1.95A)

DESIGN NOTE:
If i.MX6DQP (the new PLUS version of CPU) is used, maximum current of +1V375_SOC increases up to 3.4A.
In this case, use separate power source U30 instead of SW1C (do not fit L8 and R384).

DESIGN NOTE:
+3V3 power rail - SW2
+3.3V / Required 2A
max 2A (peak 2.1A)

DESIGN NOTE:
+1V5_DDR power rail - SW3A/B
+1.5V / Required 2A
max 2.5A (peak 2.7A)

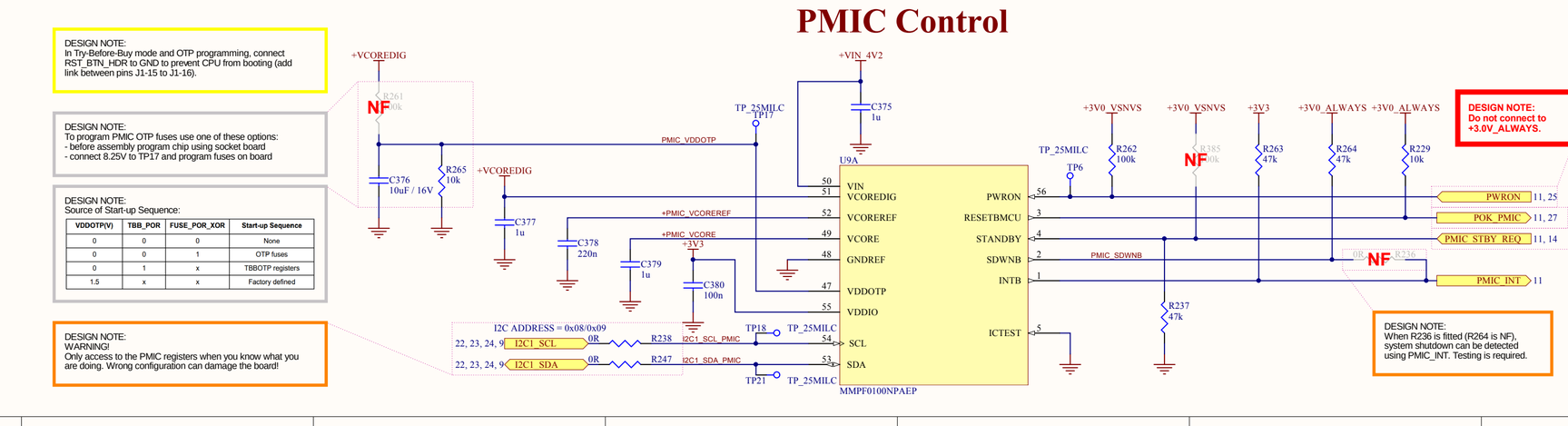
DESIGN NOTE:
+1V5_DDR current calculation
I_DDR = cpu+memories + PCIe card
= 1400mA + 500mA = 1900mA

DESIGN NOTE:
+0V75_DDR_VTT power rail - SW4
+0.75V / Required 0.4A
max 1A (peak 1A)

DESIGN NOTE:
SW4 regulator needs to be set up to VTT mode (set bit VTT to 1 in OTP_SW4_CONF register).

DESIGN NOTE:
+5V power rail - SWBST
+5V / Required 0.6A
max 0.6A (peak 1.4A)

PMIC Control



DESIGN NOTE:
In Try-Before-Buy mode and OTP programming, connect RST_BTN_HDR to GND to prevent CPU from booting (add link between pins J1-15 to J1-16).

DESIGN NOTE:
To program PMIC OTP fuses use one of these options:
- before assembly program chip using socket board
- connect 8.25V to TP17 and program fuses on board

DESIGN NOTE:
Source of Start-up Sequence:

VDDOTP(V)	TBB_POR	FUSE_POR_XOR	Start-up Sequence
0	0	0	None
0	0	1	OTP fuses
0	1	x	TBBOTP registers
1.5	x	x	Factory defined

DESIGN NOTE:
WARNING!
Only access to the PMIC registers when you know what you are doing. Wrong configuration can damage the board!

DESIGN NOTE:
When R236 is fitted (R264 is NF), system shutdown can be detected using PMIC_INT. Testing is required.

DESIGN NOTE:
Do not connect to +3.0V_ALWAYS.

DESIGN NOTE:
PMPF0100 Revision 1.0 through Revision 1.2 are subject to boot issues if power is removed from the board and reapplied within 2 minutes. PMPF0100 Revison 2.0 will correct this issue. For more details, see the PMPF0100 ERRATA, Issue #ER19

Be sure you always use the Revision which fixes this isssue!

DESIGN NOTE:
Setup fault mode for POK_PMIC operation. Testing is required.

DESIGN NOTE:
When Standby is generated by CPU / MCU do not fit R237 and fit R385, D28 & D36.

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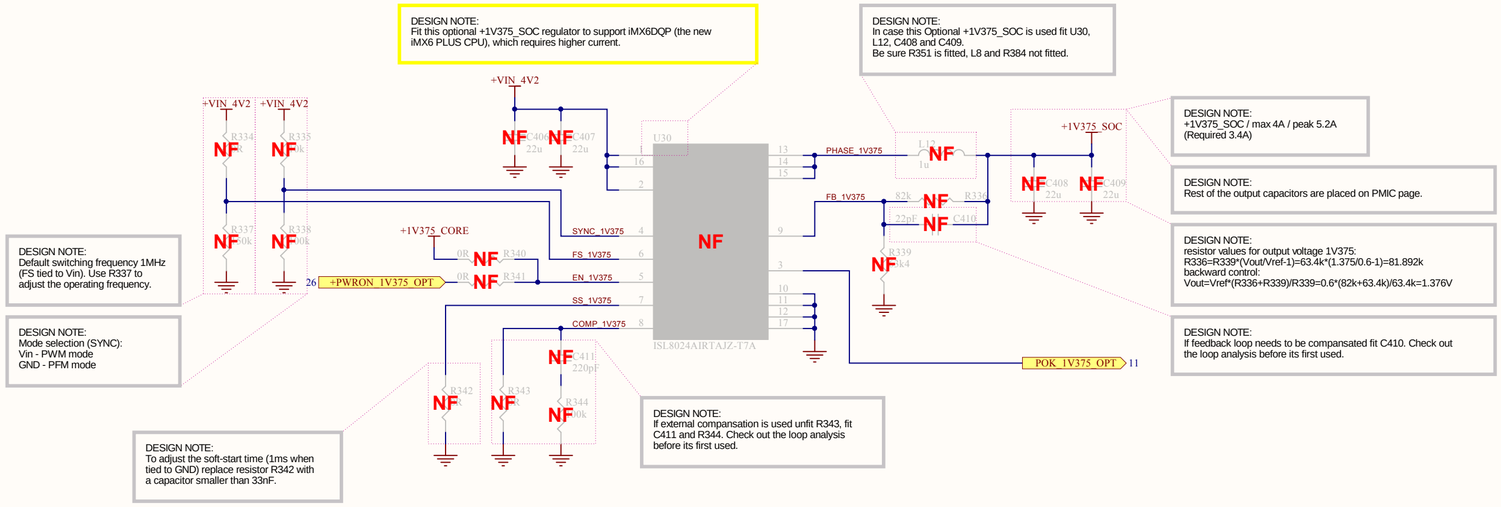
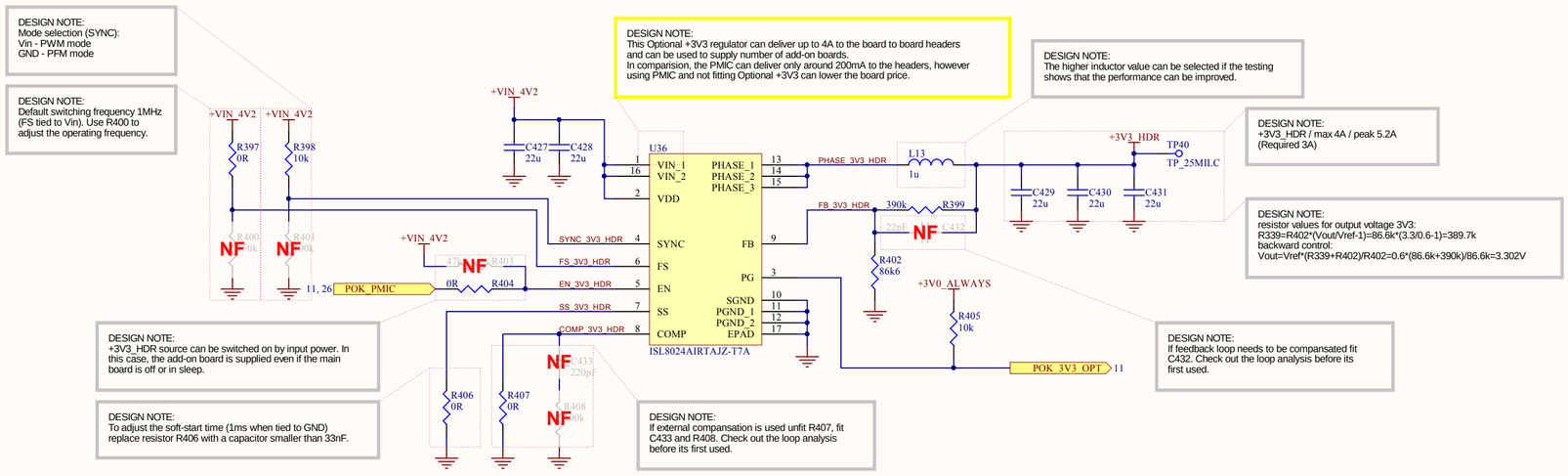
PWR +1V375_SOC OPT, +3V3 OPT

Optional +1V375_SOC



Optional +3V3



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Title: OpenRex		Variant: Production	
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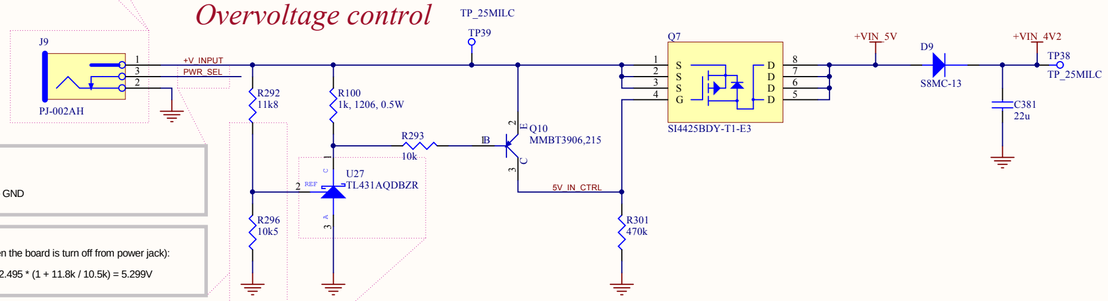
PWR IN, MECHANICAL, DOC

Power Input (+5V DC)

DESIGN NOTE:
Input voltage (+VIN_5V): +4.9 - 5.2V
Required max. current 7.5A (max. 5.5A through D9)

DESIGN NOTE:
J9 maximum current is 5A.

Overvoltage control



DESIGN NOTE:
Power jack connector insertion switch:
Jack plugged in - PWR_SEL high Z
Jack removed - PWR_SEL connected to GND

DESIGN NOTE:
Reference voltage (the input voltage when the board is turn off from power jack):
V_out_off = 5.3V; V_ref = 2.495V
V_out_off = V_ref * (1 + R292 / R296) = 2.495 * (1 + 11.8k / 10.5k) = 5.299V

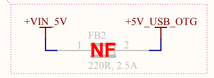
DESIGN NOTE:
Chip U27 is a shunt regulator and is used to control the overvoltage protection.

When the voltage on divider R292-R296 is below internal reference (+V_INPUT is lower then 5.3V), then input voltage is connected to the system input power (+VIN_5V).

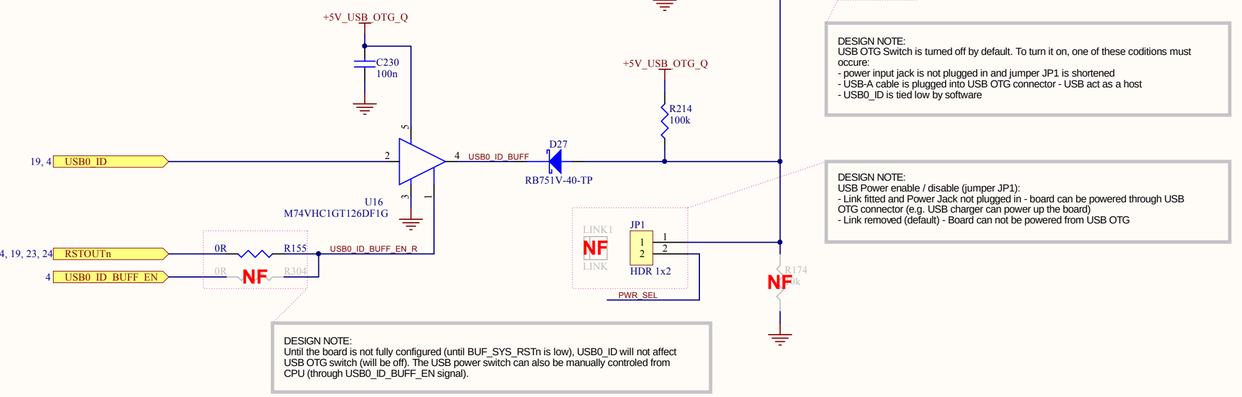
If +V_INPUT is above +5.3V, transistor Q7 is turn off to protect the board.

USB0 OTG Power Switch

DESIGN NOTE:
Fit FB2 if USB OTG power detection is not needed or if USB connector is the only option for supply the board (e.g. min. configuration).



USB switch control



DESIGN NOTE:
USB OTG Switch is turned off by default. To turn it on, one of these coditions must occure:
- power input jack is not plugged in and jumper JP1 is shortened
- USB-A cable is plugged into USB OTG connector - USB act as a host
- USB0_ID is tied low by software

DESIGN NOTE:
USB Power enable / disable (jumper JP1):
- Link fitted and Power Jack not plugged in - board can be powered through USB OTG connector (e.g. USB charger can power up the board)
- Link removed (default) - Board can not be powered from USB OTG

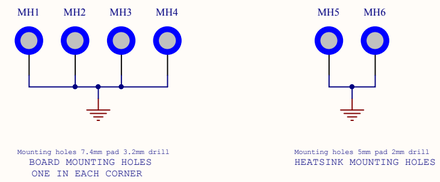
DESIGN NOTE:
Until the board is not fully configured (until BUF_SYS_RSTn is low), USB0_ID will not affect USB OTG switch (will be off). The USB power switch can also be manually controled from CPU (through USB0_ID_BUFF_EN signal).

License

I2C USAGE AND ADDRESS TABLE

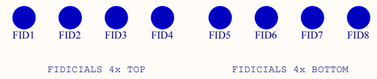
NAME	PERIPHERAL	ADDRESS
I2C1	*PMIC control*	*0x08 / 0x09*
	Compass + Accelerometer	*0x38 / 0x39*
	Gyroscope	*0x40 / 0x41*
	EEPROM	*0xAE / 0xAF*
	MCU (LPC13xx)	
	For general use (on header J1)	
I2C2	*Audio*	*0x14 / 0x15*
	HDMI	*0x60 , 0xA1*
	Humidity sensor	*0x80 / 0x81*
	Temperature sensor	*0x90 / 0x91*
	Mini PCIe Card	
	CSI / LVDS Connector	
	For general use (on header J2)	
I2C3	*DISP0 / CSI1 Connector*	
	For general use (on header J2)	

Mounting Holes



PCB

Fiducials



Gnd Testpoint

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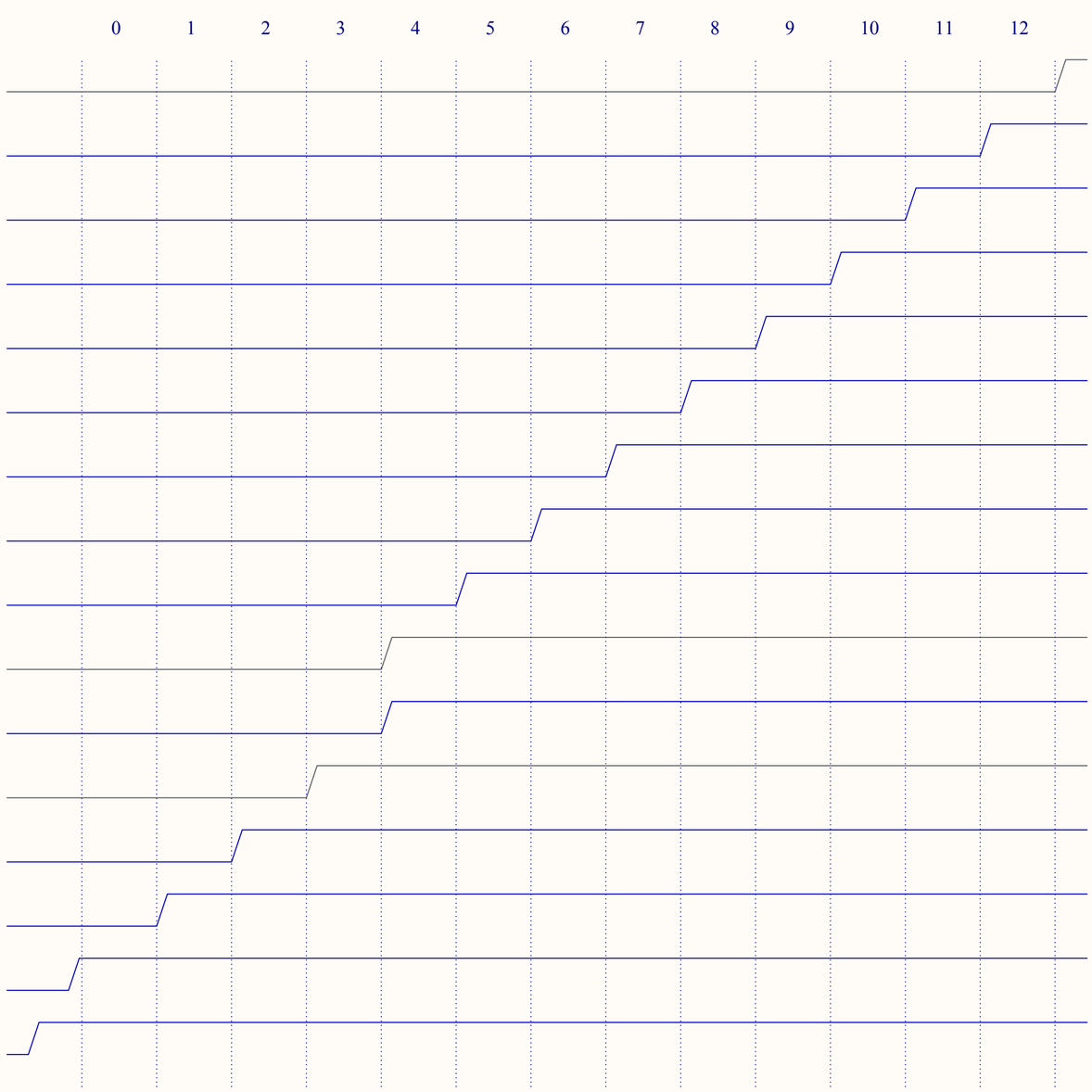
POWER SEQUENCING

FROM	OTHER POWERS	LEVEL	USED BY
VGEN5	+3V3_LDO	3.3V	MCU (optional)
PMIC	+DDR_VREF	0.75V	ref. for DDR memories (from +1V5_DDR)
CPU	+1V2_VDD_ARM_CAP	0.950 - 1.25V	core caps, CPU
CPU	+1V1_VDDSOC_CAP	1.175 - 1.25V	core caps, CPU-sata, CPU-pcie, CPU-hdmi
CPU	+VDDPU	1.175 - 1.25V	core caps

PMIC NAME / CHIP	NAME	LEVEL	USED BY
U32 (page 15)	+1V2_REG	1.2V	ethernet phy (optional)
U36 (page 27)	+3V3_HDR	3.3V	headers
VGEN3	+1V8_AUDIO	1.8V	audio codec
VGEN2	+1V2_PMIC	1.2V	ethernet phy
SWBST	+5V	5V	CPU, chips, headers
VGEN4	+2V5	2.5V	CPU, ethernet phy
SW2	+3V3	3.3V	CPU, chips, peripherals
SW4	+0V75_DDR_VTT	0.75V	memories termination
SW3AB	+1V5_DDR	1.5V	CPU, memories
U30 (page 27)	+1V375_SOC	1.375V	CPU core voltage (optional from U30)
SW1C	+1V375_SOC	1.375V	CPU core voltage (default from PMIC)
VGEN1	+PWRON_OPT_1V375	1.2V	Enable signal for +1V375_SOC chip U30 (opt., not used as a power)
SW1AB	+1V375_CORE	1.375V	CPU core voltage
VGEN6	+3V0_ALWAYS	3.0V	CPU, reset buffer, CPU config
VSNVS	+3V0_VSNVS	3.0V	PMIC PWRON
	+VIN	4.8V-5.3V	PMIC, USB connectors, headers

POWER UP SEQUENCE



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REVISION HISTORY

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Designator
[01] - COVER PAGE.SchDoc

Designator
[02] - BLOCK DIAGRAM.SchDoc

Designator
[03] - CPU - DDR3, DDR3 MEM.SchDoc

Designator
[04] - CPU - PCIE, USB.SchDoc

Designator
[05] - CPU - HDMI, LVDS.SchDoc

Designator
[06] - CPU - ETHERNET, SATA.SchDoc

Designator
[07] - CPU - CSI, DISP.SchDoc

Designator
[08] - CPU - SPI, UART.SchDoc

Designator
[09] - CPU - SD, AUDIO, I2C, CAN.SchDoc

Designator
[10] - CPU - GPIO, PWM, LEDS, BUTTONS.SchDoc

Designator
[11] - CPU - JTAG, CONTROL.SchDoc

Designator
[12] - CPU - POWER.SchDoc

Designator
[13] - CPU - UNUSED.SchDoc

Designator
[14] - MCU.SchDoc

Designator
[15] - ETHERNET PHY.SchDoc

Designator
[16] - HDMI.SchDoc

Designator
[17] - LVDS, CSI, LCD, TSC.SchDoc

Designator
[18] - PCIE MINI.SchDoc

Designator
[19] - USB.SchDoc

Designator
[20] - ETHERNET, SATA.SchDoc

Designator
[21] - AUDIO.SchDoc

Designator
[22] - SD CARD, SPI, FLASH, EEPROM, .SchDoc

Designator
[23] - SENSORS, CAN, IR.SchDoc

Designator
[24] - HEADERS, UART.SchDoc

Designator
[25] - LEDS, BUTTONS.SchDoc

Designator
[26] - PWR PMIC.SchDoc

Designator
[27] - PWR 1V375 OPT, 3V3 OPT.SchDoc

Designator
[28] - PWR IN, MECH, DOC.SchDoc

Designator
[29] - POWER SEQUENCING.SchDoc

Designator
[30] - REVISION HISTORY.SchDoc

NOTES

Mark Not Fitted Components as
NF

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

Title:	OpenRex	Variant: Production	
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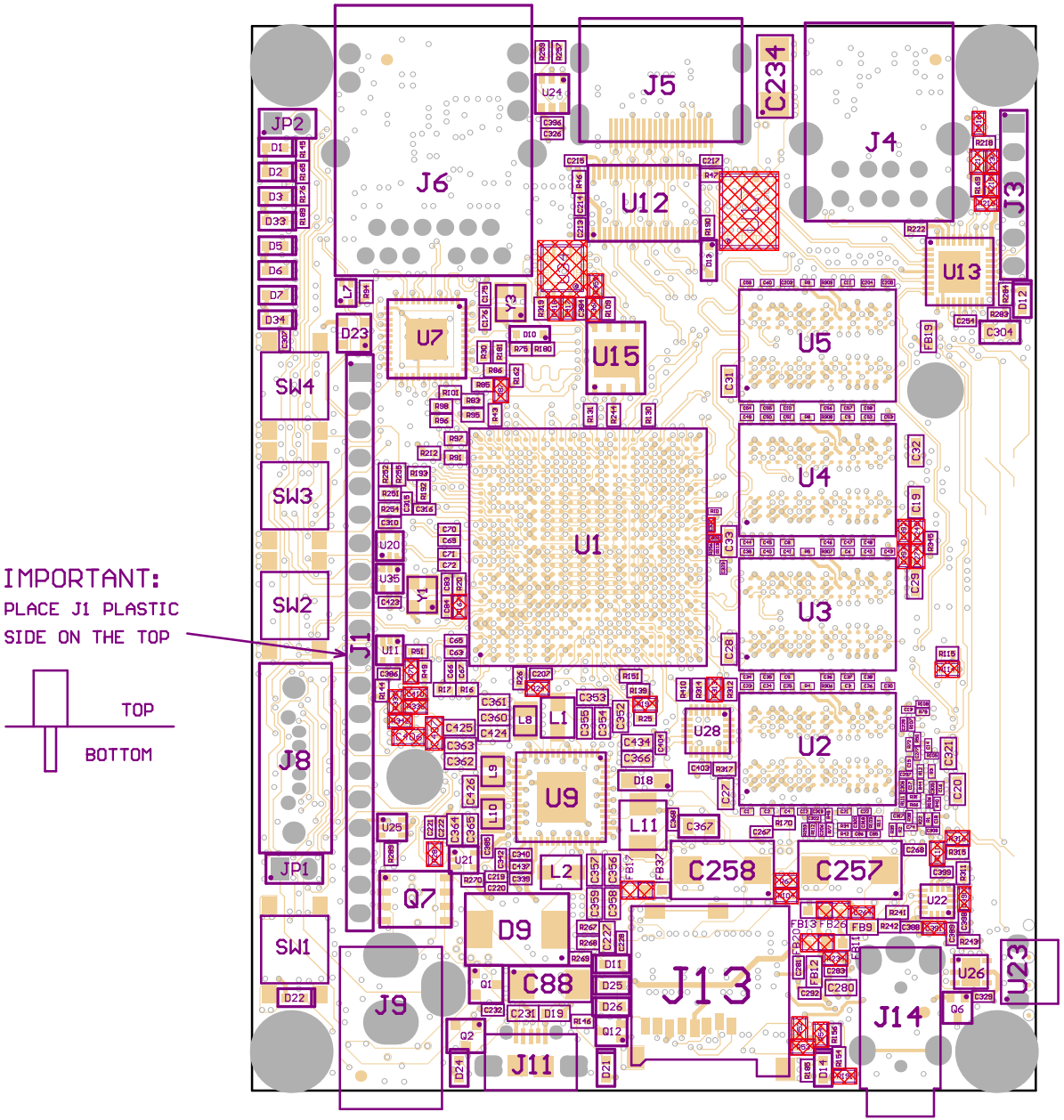
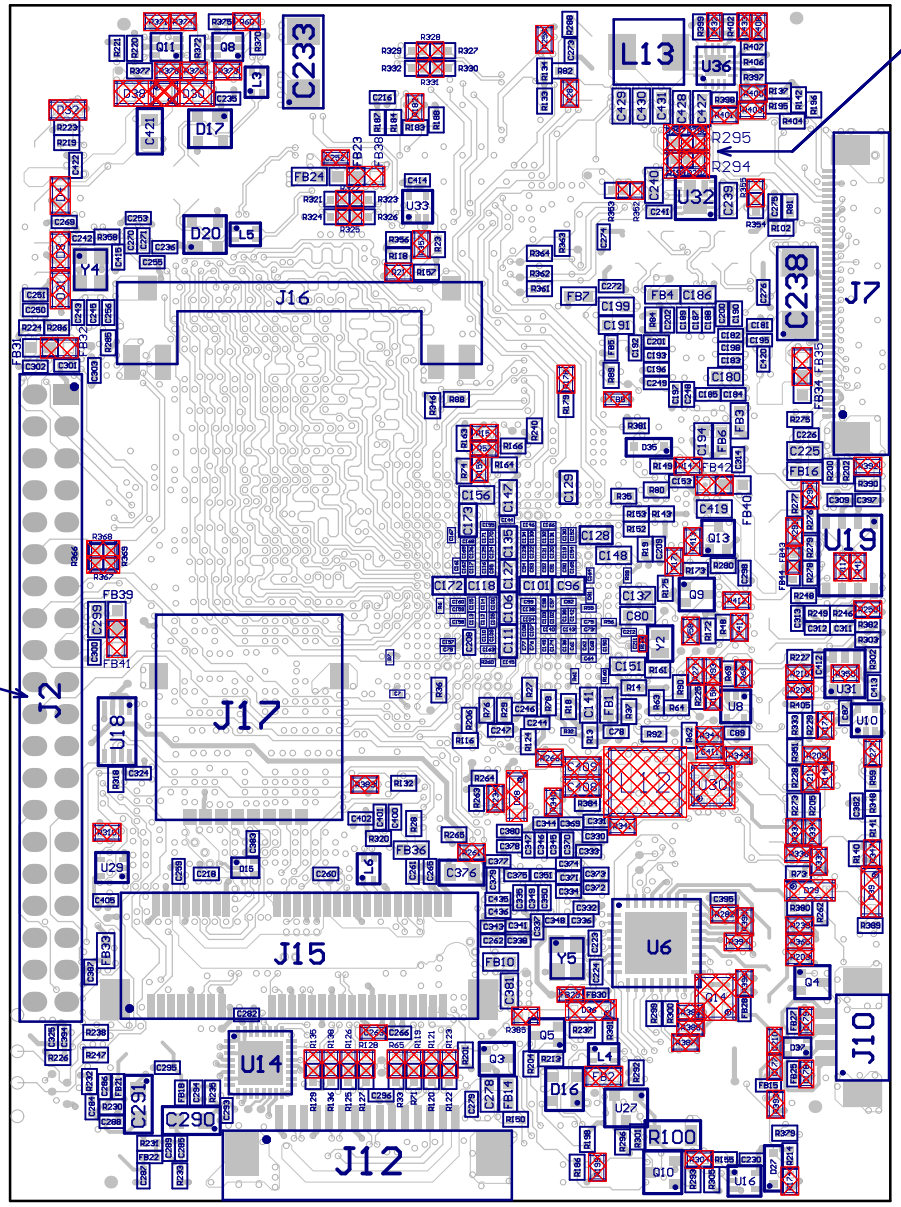
Assembly TOP of OpenRex V1I1

Production



Assembly BOTTOM of OpenRex V1I1

Production



FITTING OPTION 1

FIT 2X 0402

FITTING OPTION 2

FIT 2X 0402

FITTING OPTION 3

FIT 2X 0805

IMPORTANT:

PLACE J2 PLASTIC SIDE ON THE BOTTOM