

iMX6 Rex Development Baseboard

Variant: Prototype

12/3/2013
V1I1

RELEASED 03-DEC-2013

Page	Index	Page	Index	Page	Index	Page	Index
1	COVER PAGE	11	AUDIO1	21		31	
2	BLOCK DIAGRAM	12	SD CARDS	22		32	
3	CONNECTORS	13	UARTS	23		33	
4	PCIE MINI 1, PCIE	14	RTC, EEPROM, GPIO, TOUCHSC.	24		34	
5	PCIE MINI 2, AUDIO2	15	MISC, JTAG, HEADERS	25		35	
6	SATA, CFAST	16	POWERS 5V, 3V3	26		36	
7	HDMI	17	PWR IN, LEDS, BUTTONS, MECH	27		37	
8	LVDS	18	DOC, POWER SEQUENCING	28		38	
9	USB	19	REVISION HISTORY	29		39	
10	ETHERNET	20		30		40	

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational
design notes .

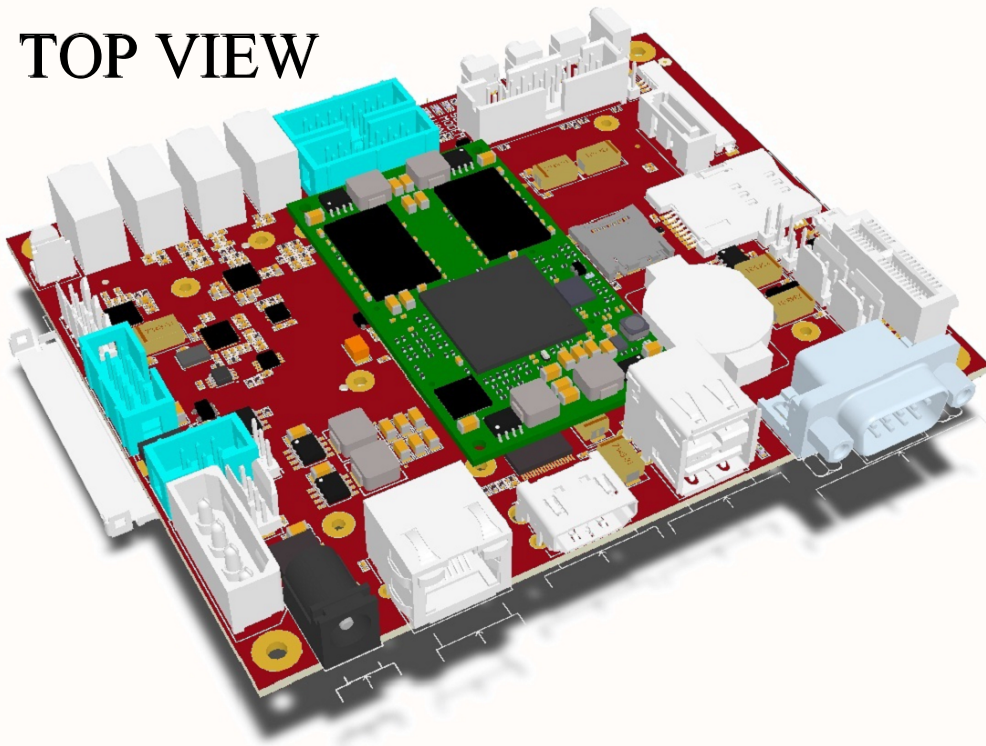
DESIGN NOTE:
Example text for cautionary
design notes.

DESIGN NOTE:
Example text for debug notes.

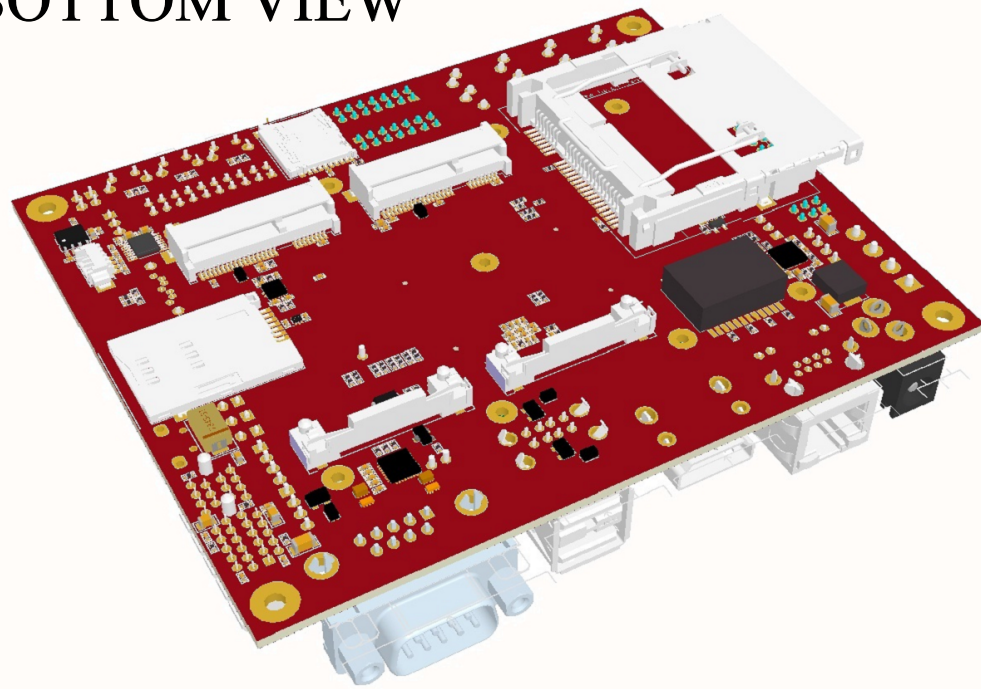
DESIGN NOTE:
Example text for critical
design notes.

LAYOUT NOTE:
Example text for critical
layout guidelines.

TOP VIEW



BOTTOM VIEW

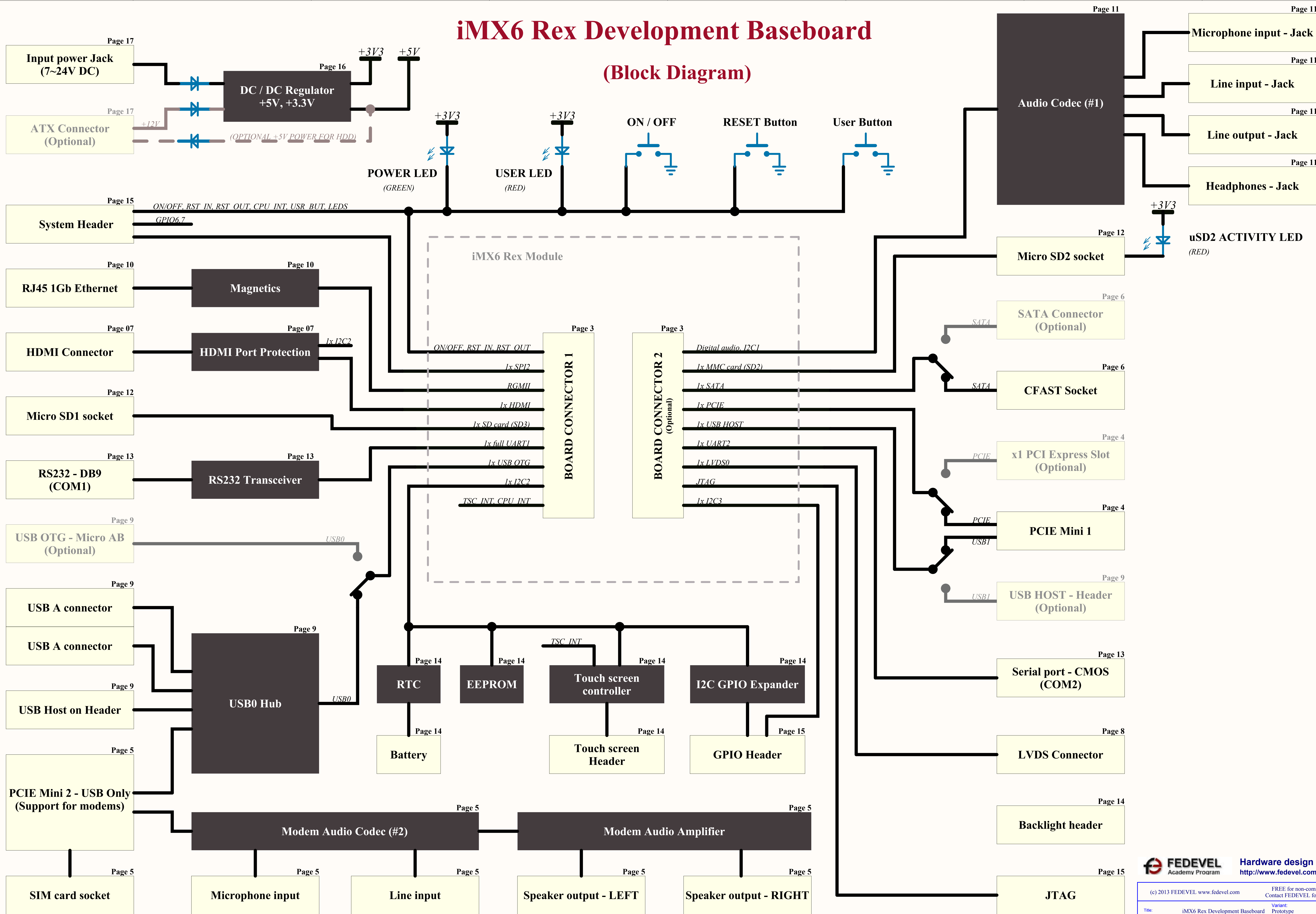


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Title:	iMX6 Rex Development Baseboard		Variant: Prototype
Page Contents:	[01] - COVER PAGE.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	12/3/2013		Sheet 1 of 20

iMX6 Rex Development Baseboard

(Block Diagram)



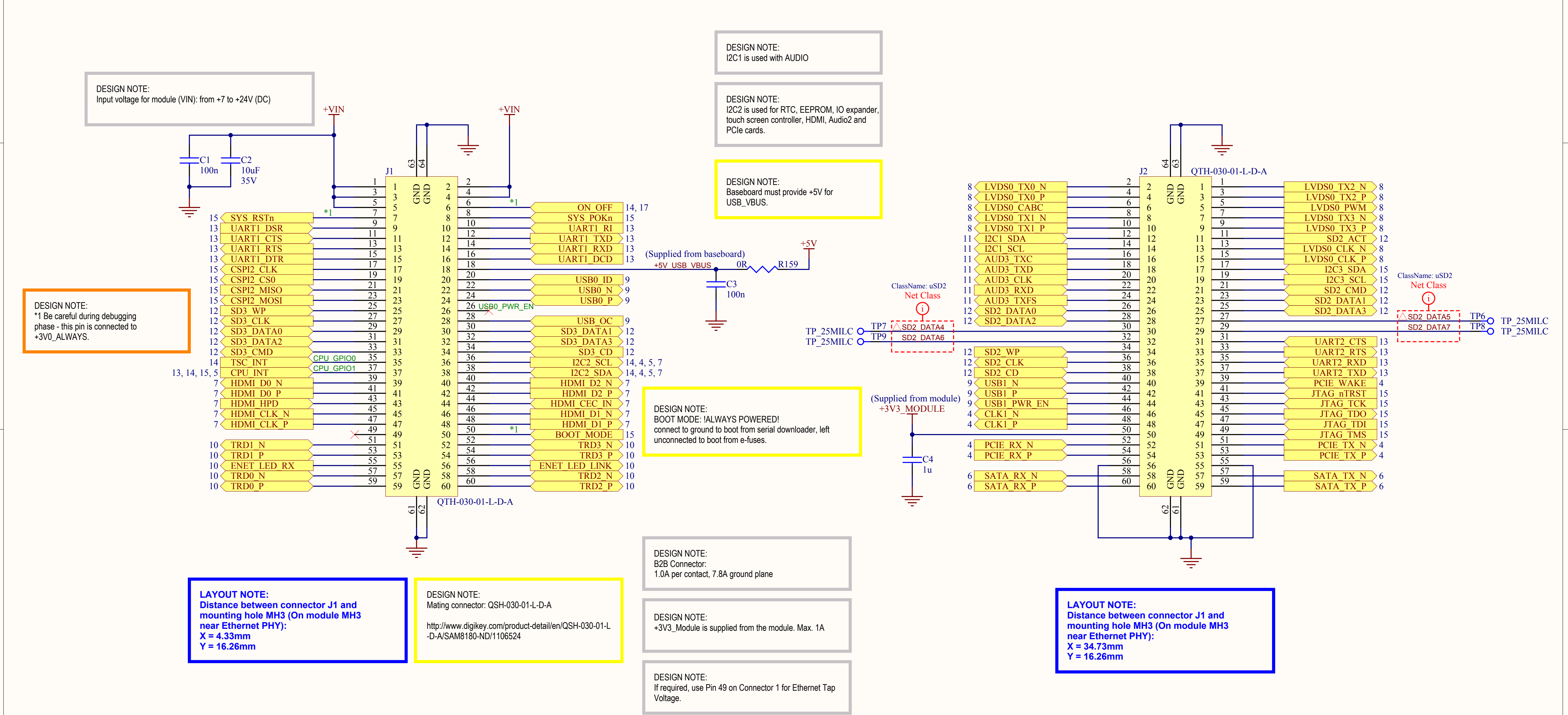
<http://www.iMX6Rex.com>



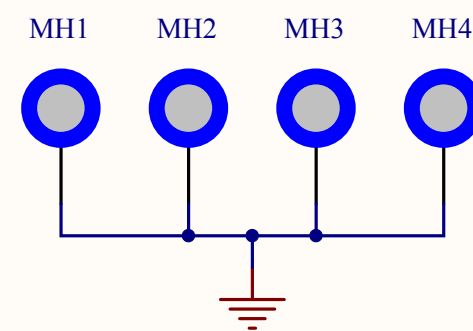
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Size:	DWG NO	Revision:	V111
Date:	12/3/2013	Sheet	2 of 20

CONNECTORS



Module Mounting Holes

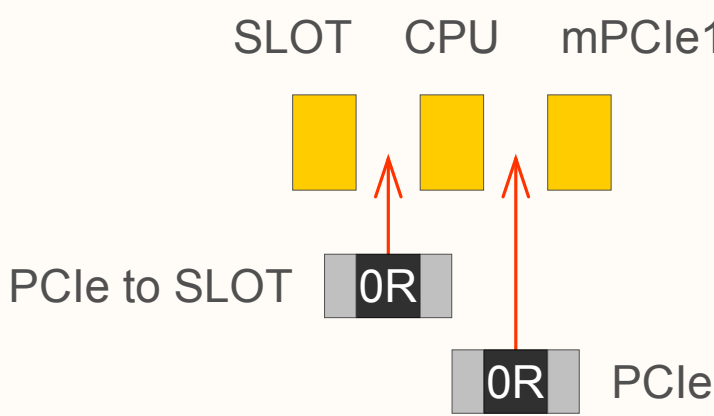
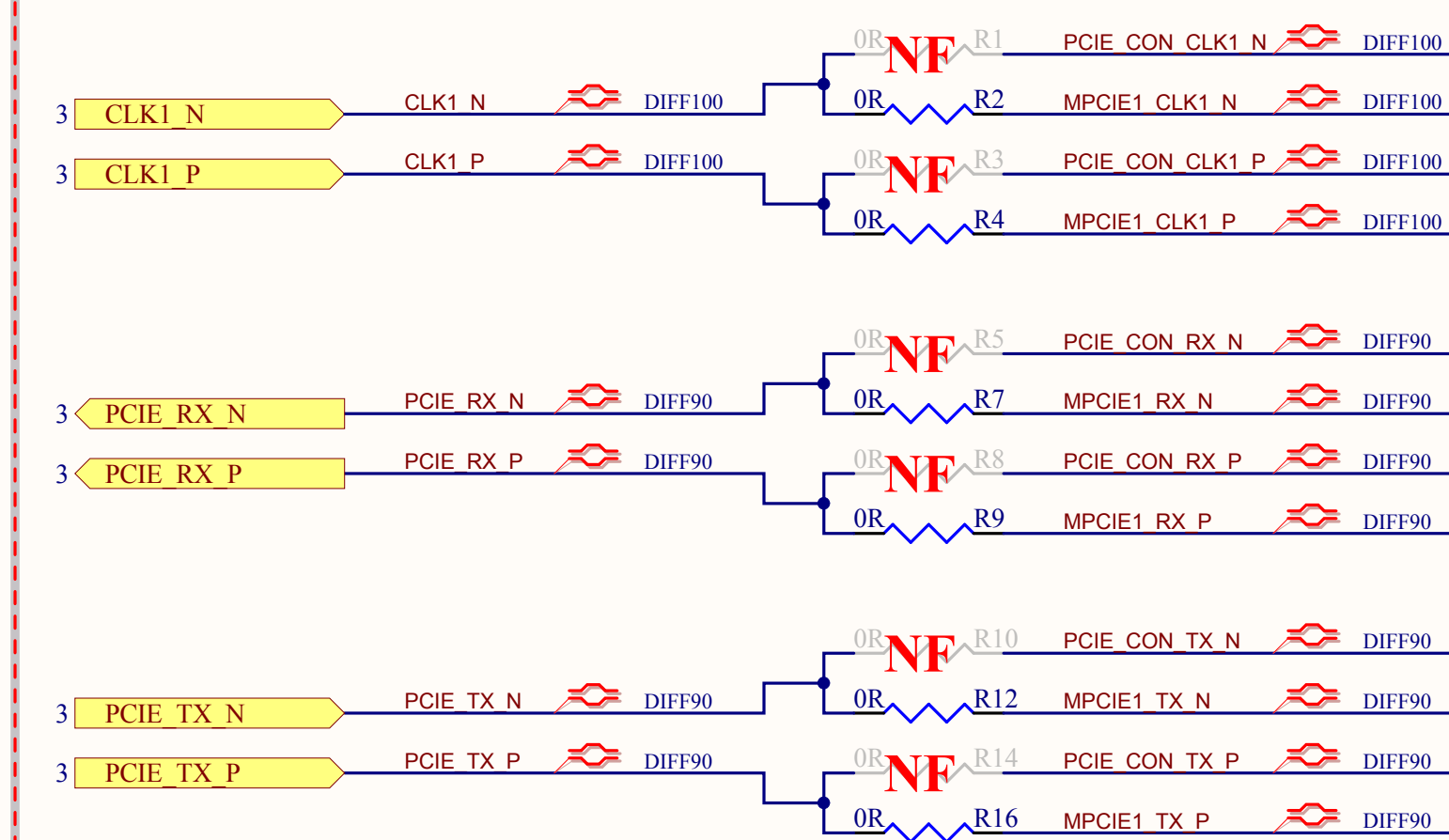


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Page Contents:	[03] - CONNECTORS.SchDoc	Checked by	
Size:	DWG NO	Revision:	V111
Date:	12/3/2013	Sheet	3 of 19

PCIE MINI 1, PCIE

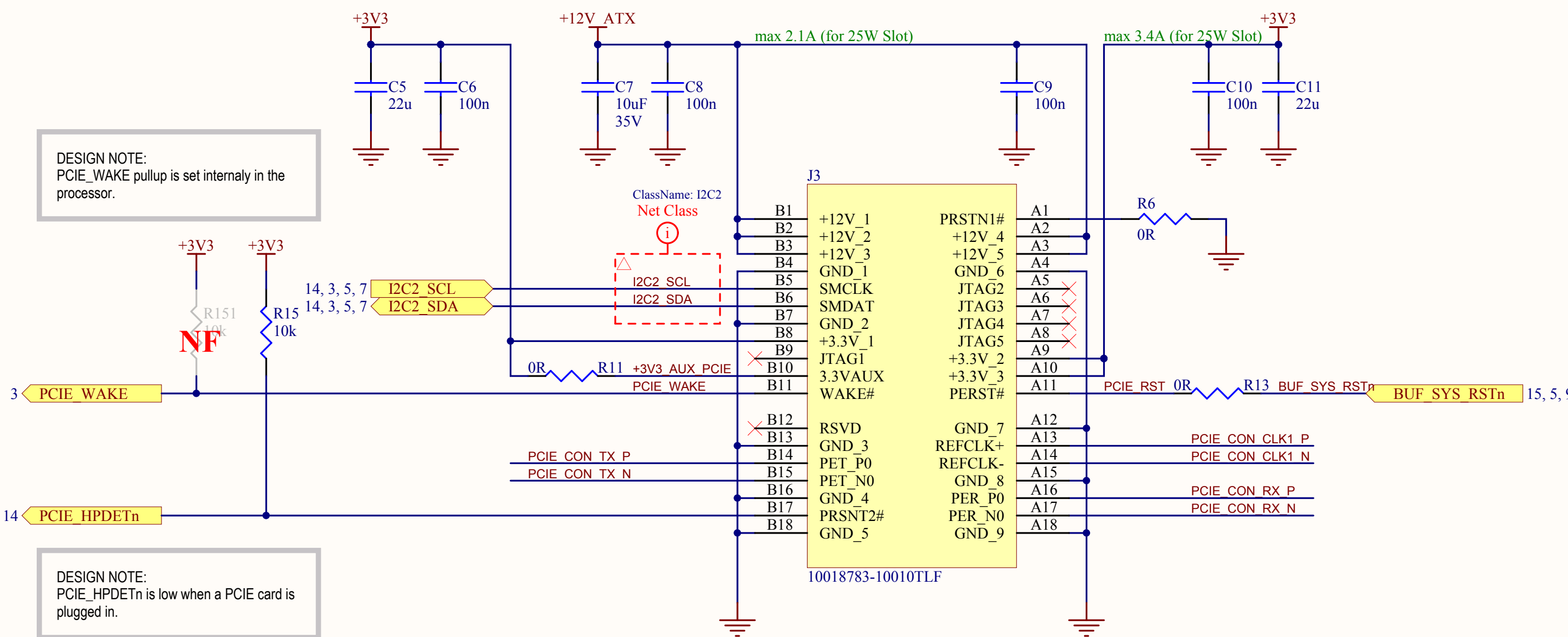
PCIE Routing



DESIGN NOTE:
Fit only one resistor per signal according to the picture below.

Net Class
ClassName: PCIE

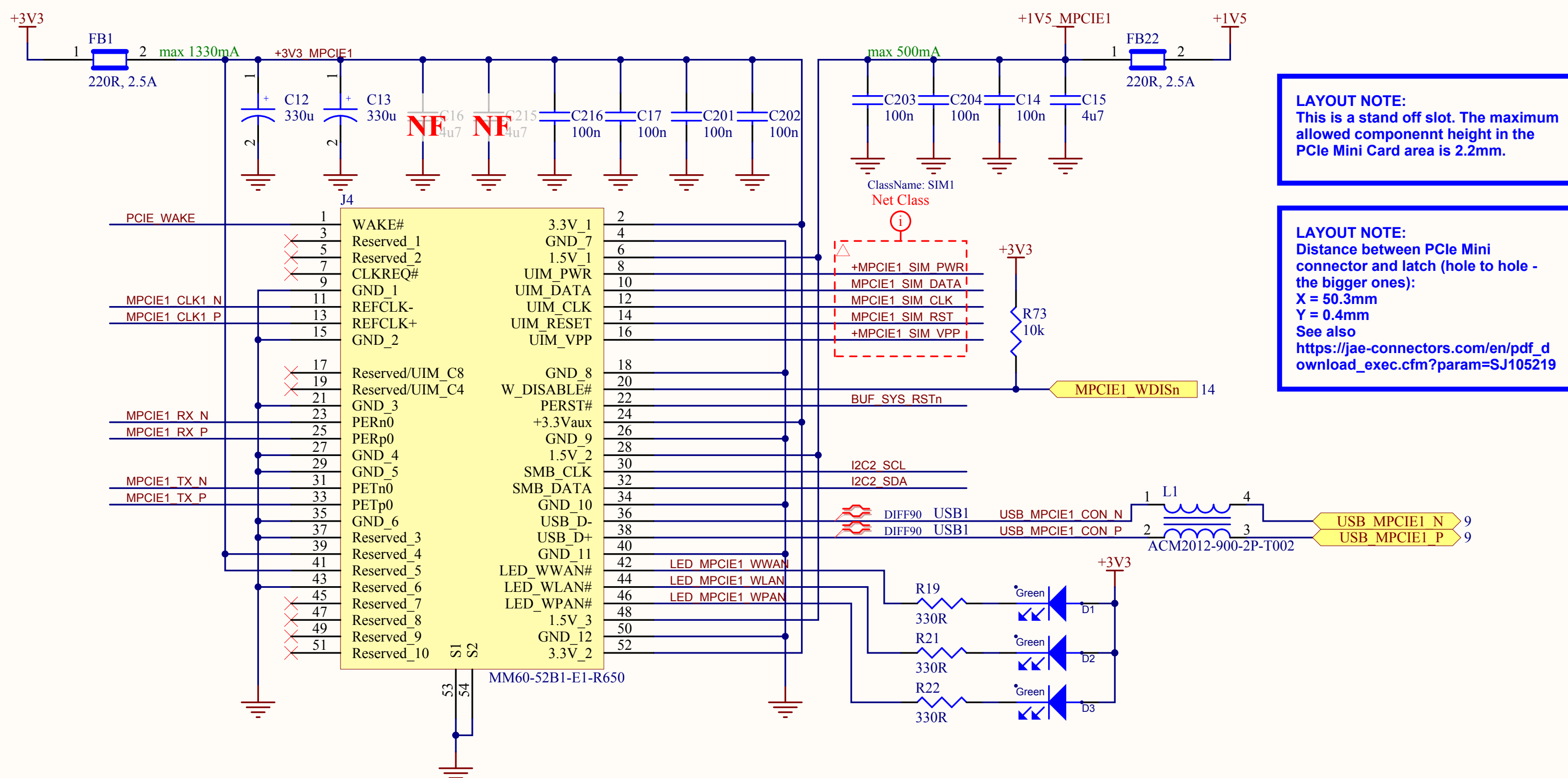
PCI Express Slot (Optional)



DESIGN NOTE:
PCIE_WAKE pullup is set internally in the processor.

DESIGN NOTE:
PCIE_HPDETn is low when a PCIE card is plugged in.

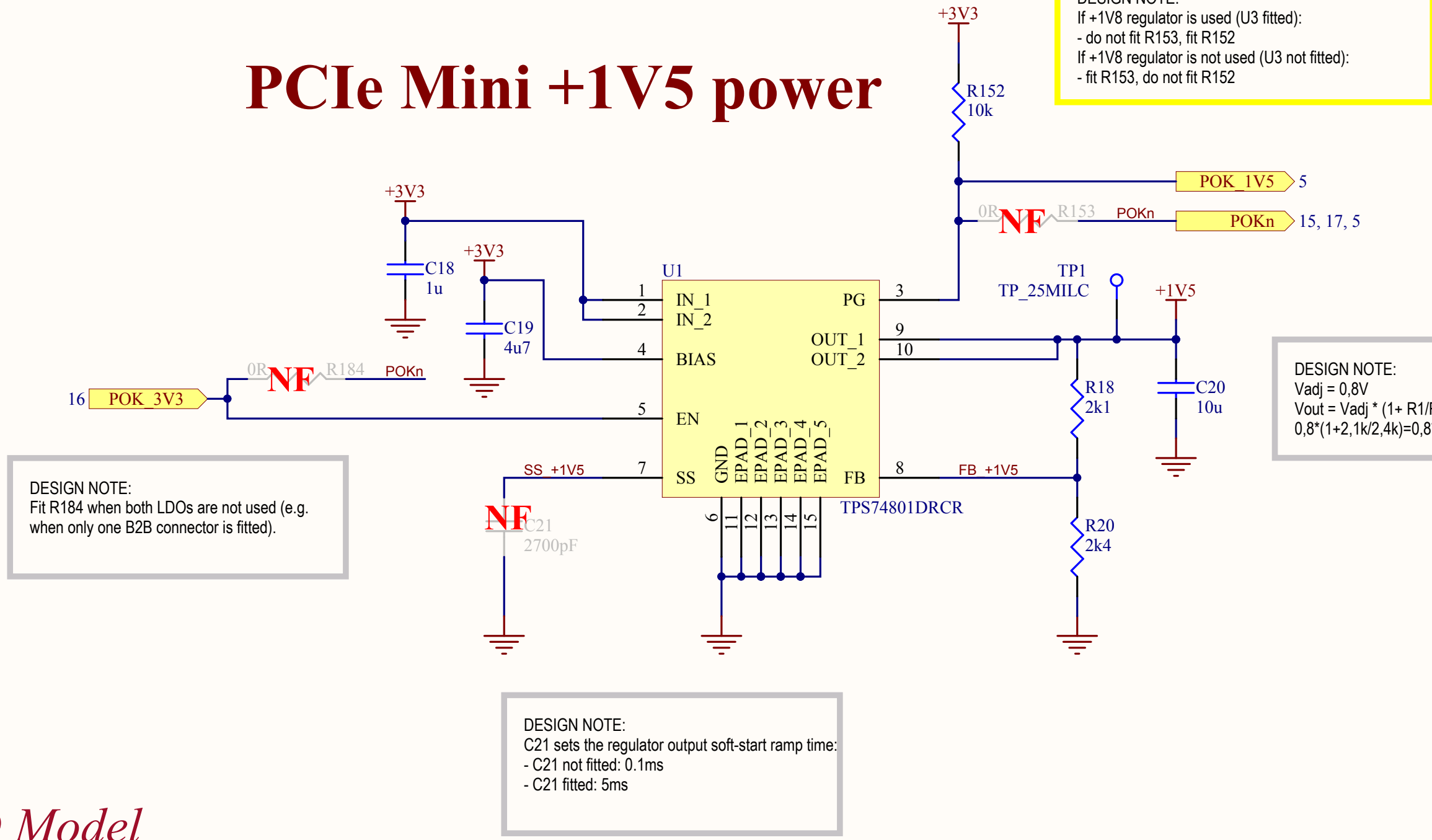
PCIE Mini 1



LAYOUT NOTE:
This is a stand off slot. The maximum allowed component height in the PCIE Mini Card area is 2.2mm.

LAYOUT NOTE:
Distance between PCIE Mini connector and latch (hole to hole - the bigger ones):
X = 60.3mm
Y = 0.4mm
See also
https://jae-connectors.com/en/pdf_download_exec.cfm?param=SJ105219

PCIE Mini +1V5 power



DESIGN NOTE:
If +1V8 regulator is used (U3 fitted):
- do not fit R153, fit R152
If +1V8 regulator is not used (U3 not fitted):
- fit R153, do not fit R152

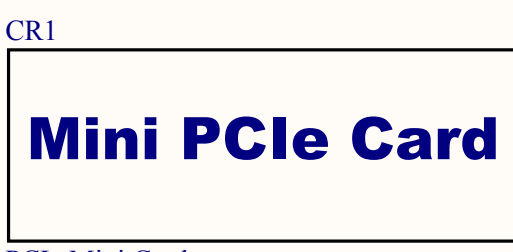
DESIGN NOTE:
Fit R184 when both LDOs are not used (e.g. when only one B2B connector is fitted).

DESIGN NOTE:
C21 sets the regulator output soft-start ramp time:
- C21 not fitted: 0.1ms
- C21 fitted: 5ms

Card Latch for PCIE Mini 1

SIM card for PCIE Mini 1

PCIE Mini 1 Card for 3D Model

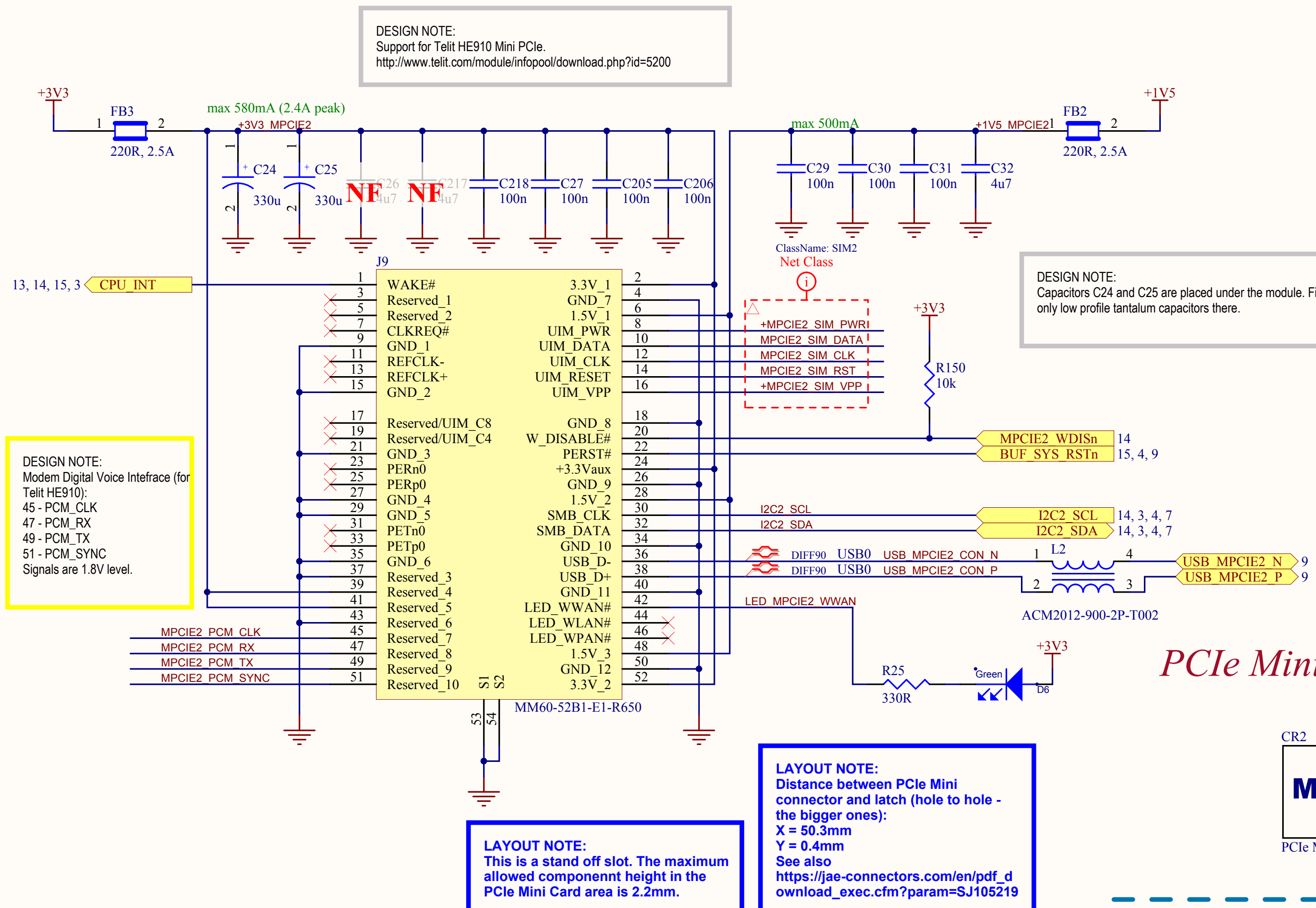


PCIE Mini Card

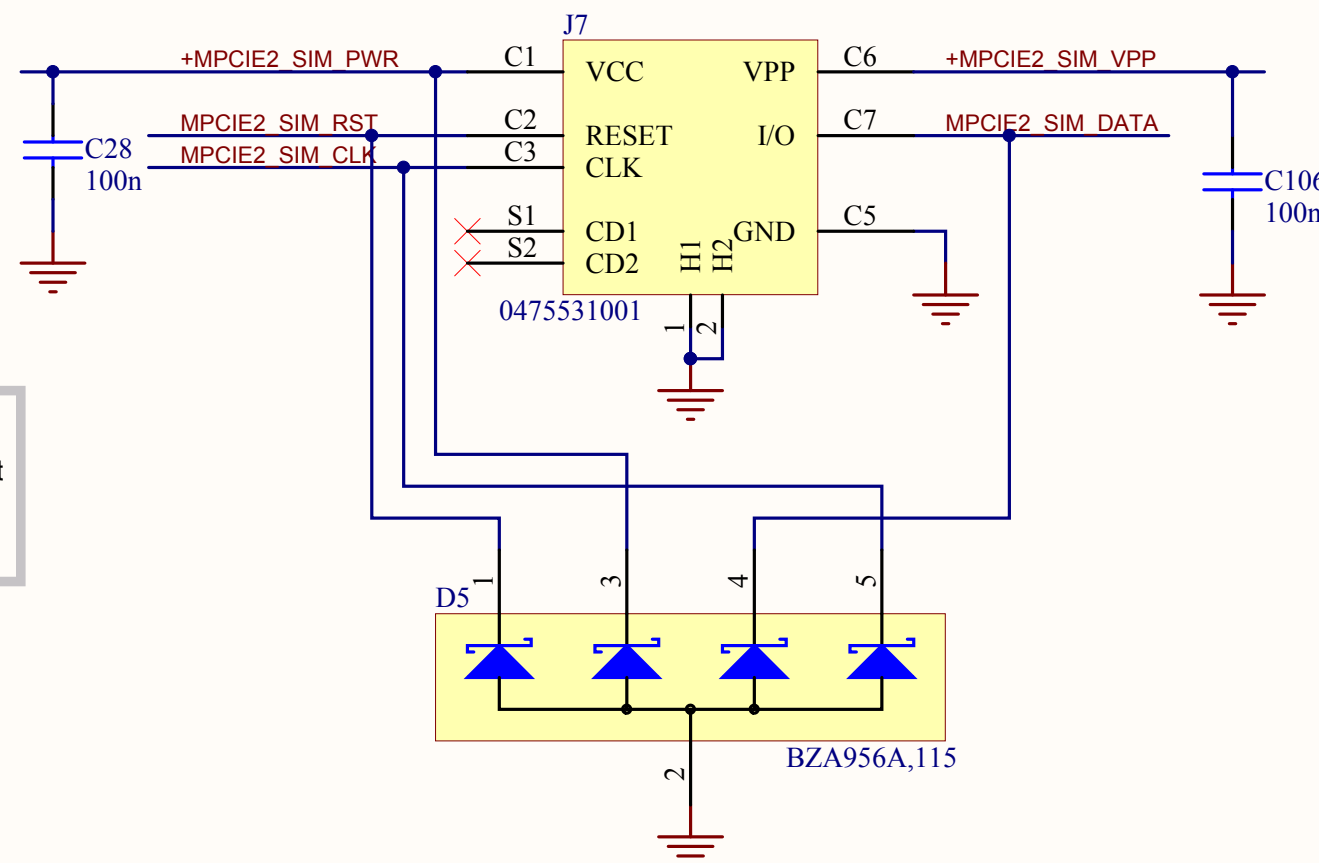
PCIE MINI 2, AUDIO2

PCIe Mini 2 - USB only

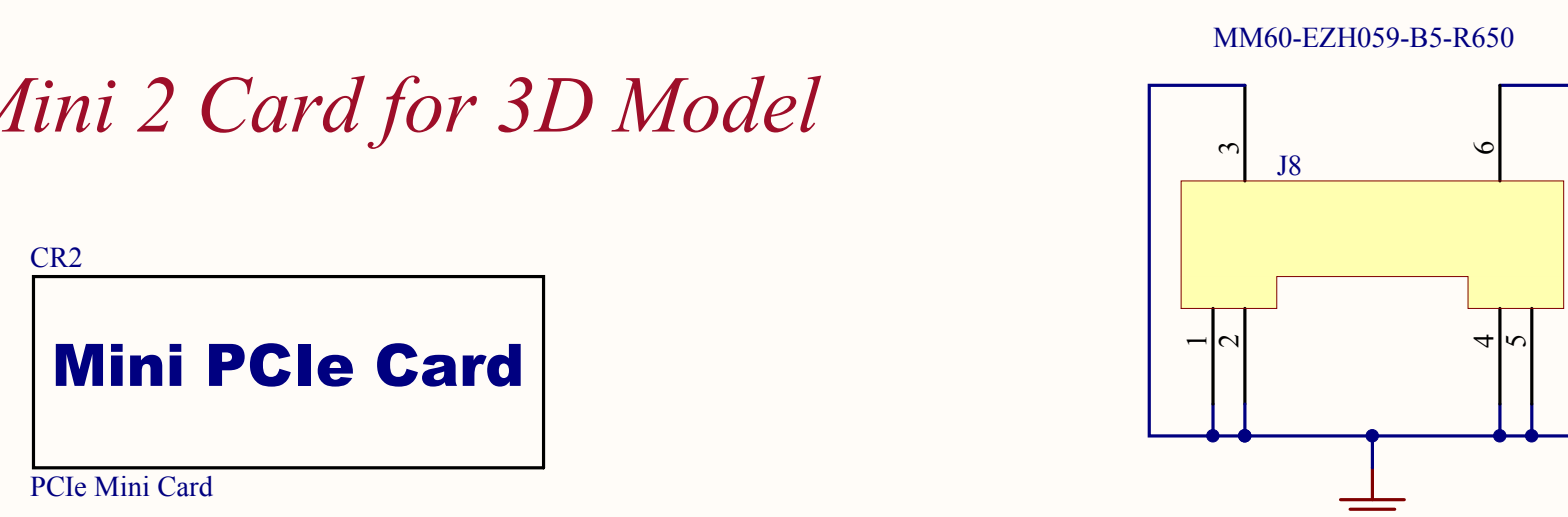
(support for wireless modems e.g GSM, 3G, ...)



SIM card for PCIe Mini 2

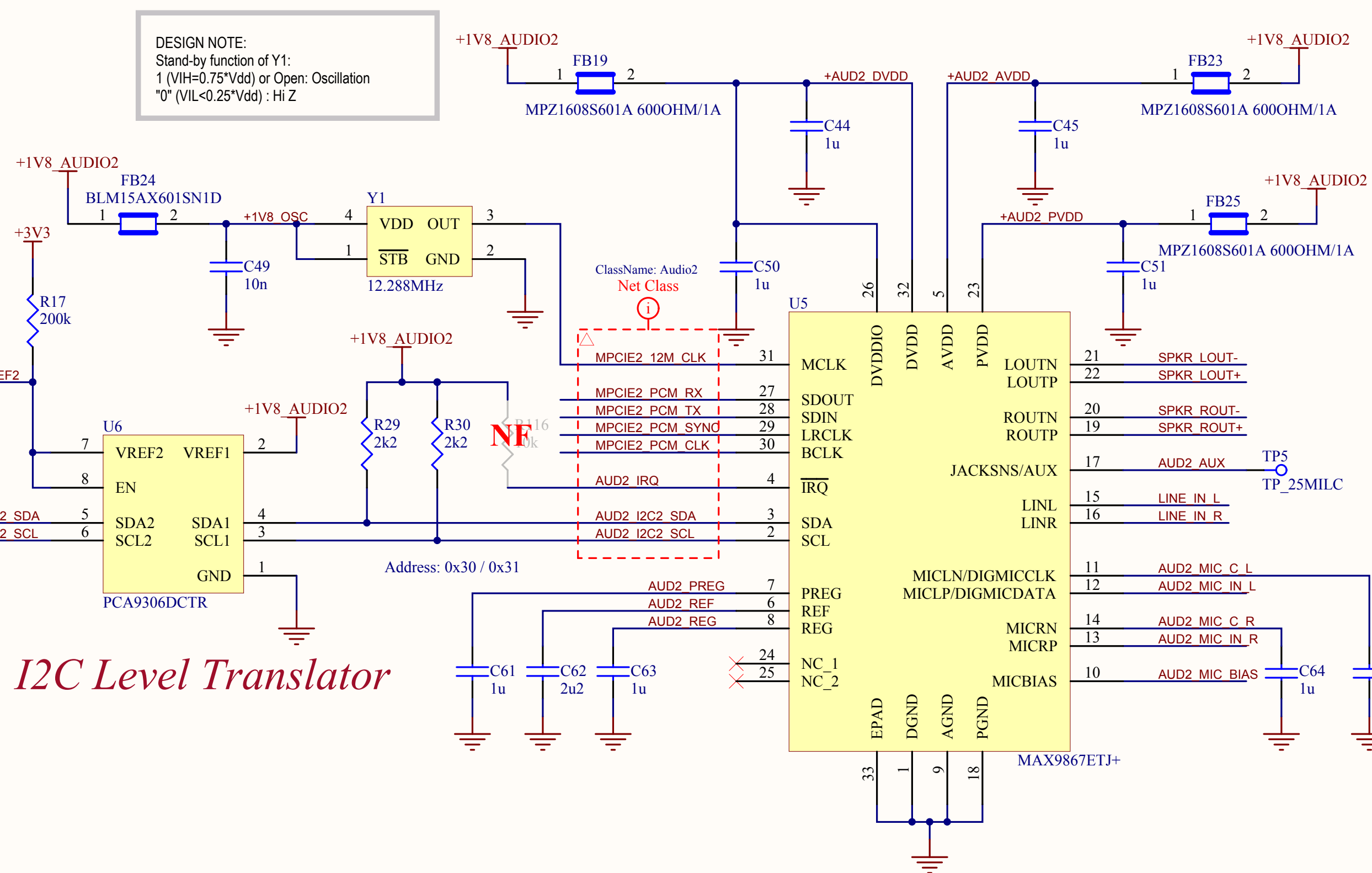


Card Latch for PCIe Mini 2

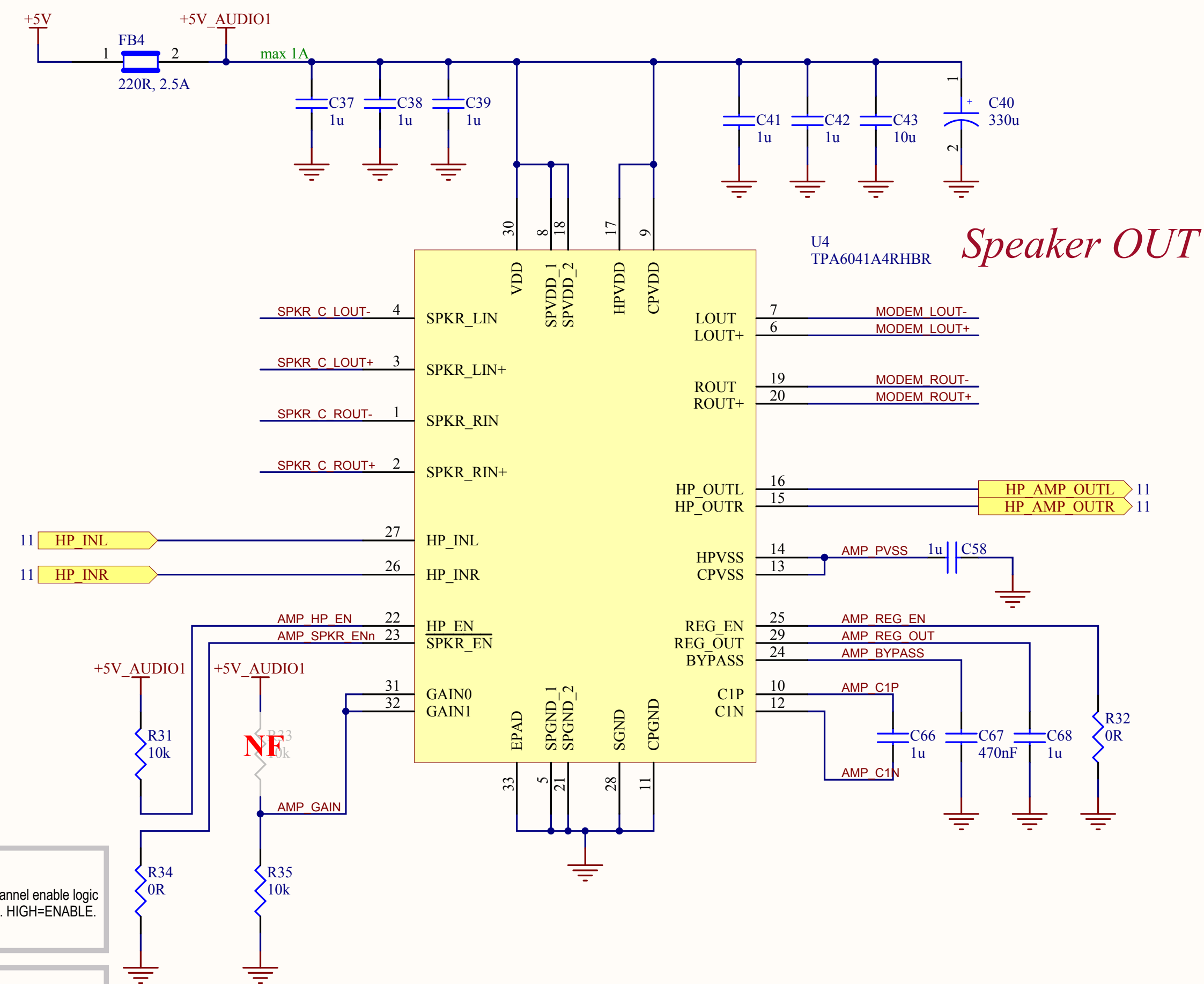


Audio 2

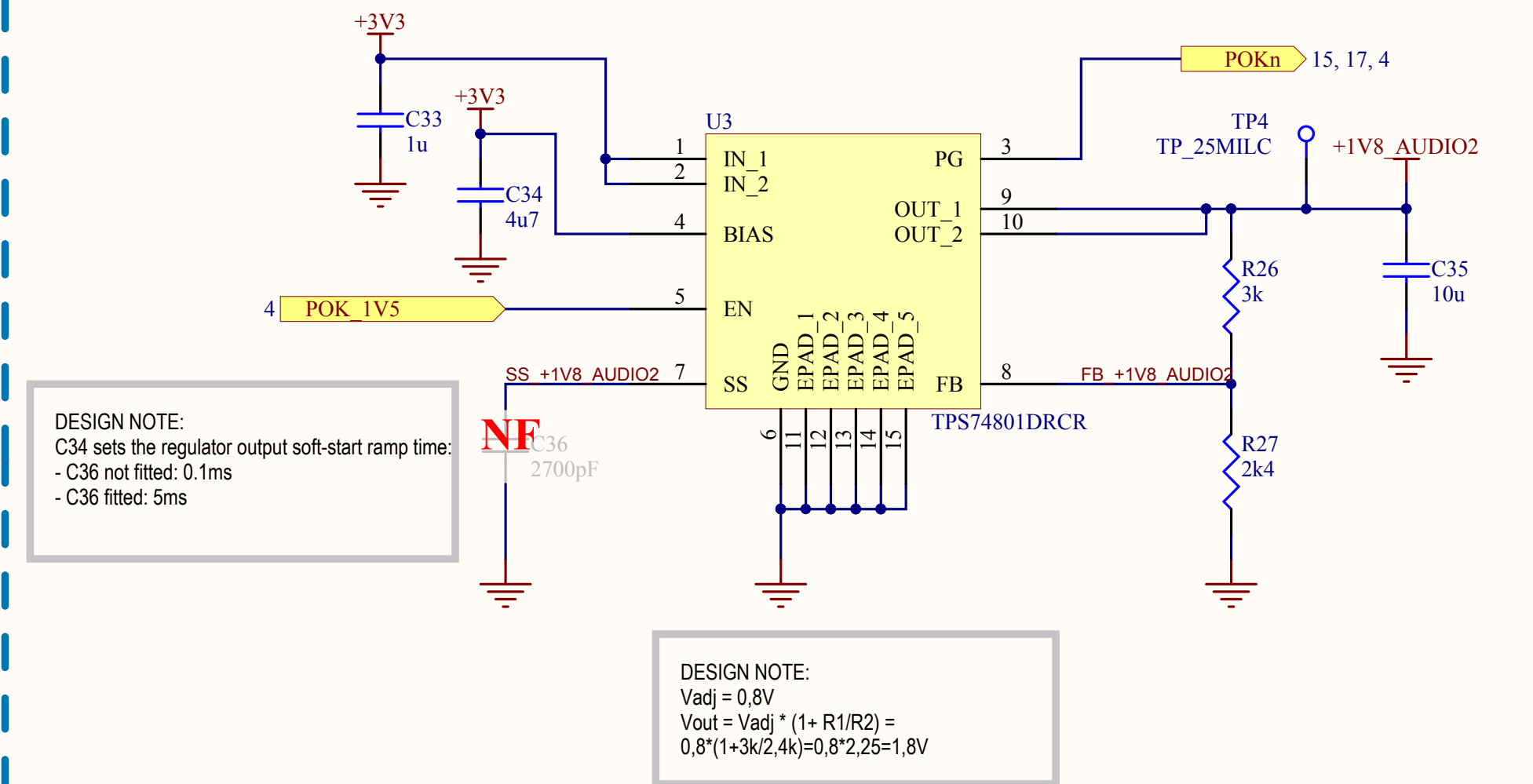
(support for wireless modem voice output / input)



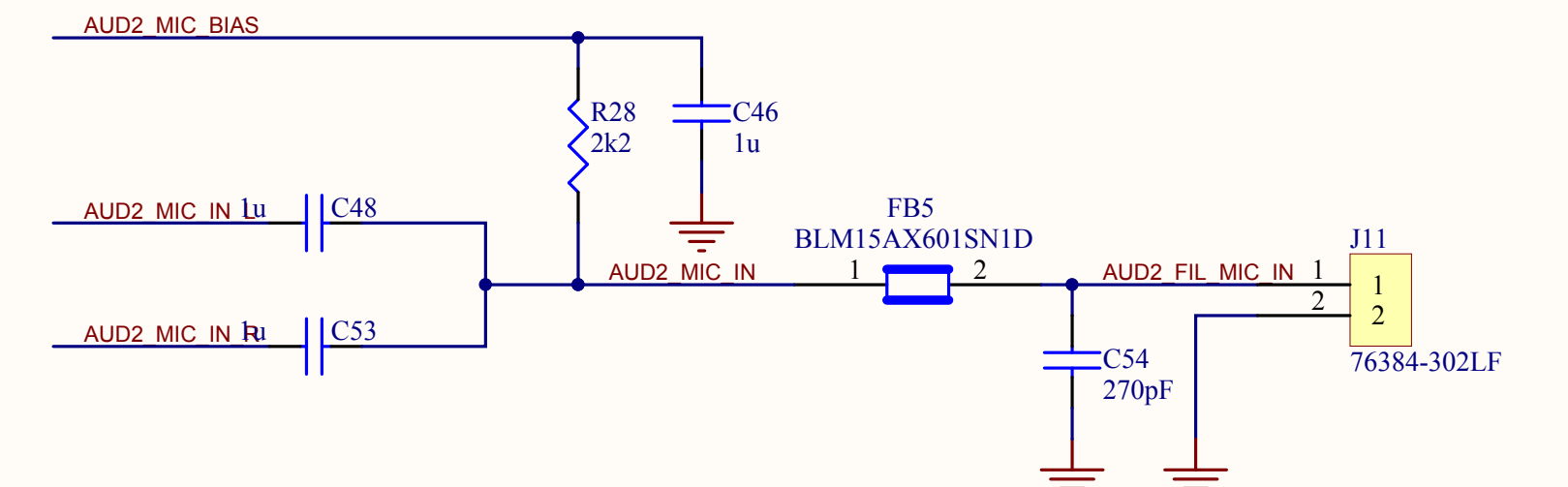
Audio Amplifier



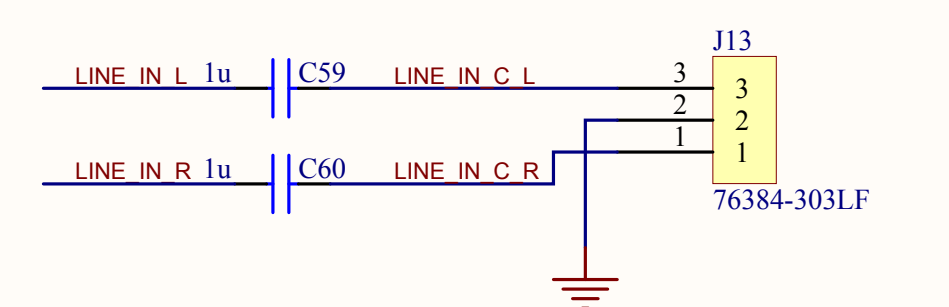
Audio2 +1V8 power



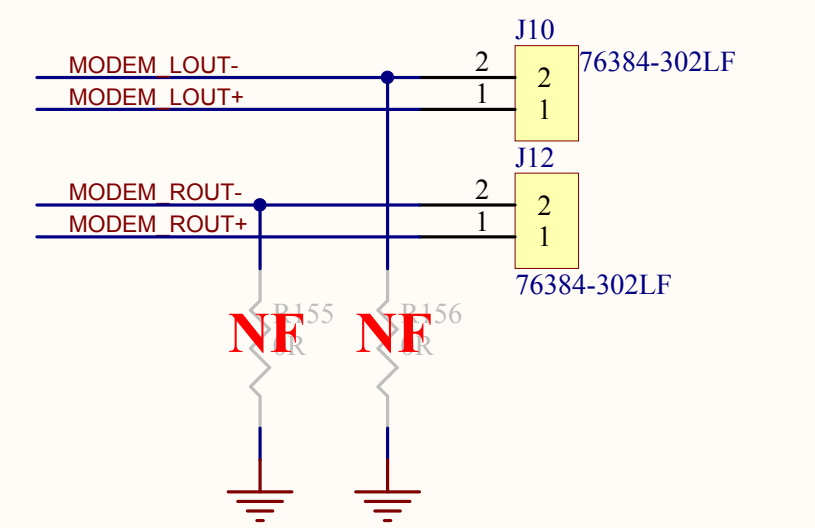
MIC IN



LINE IN



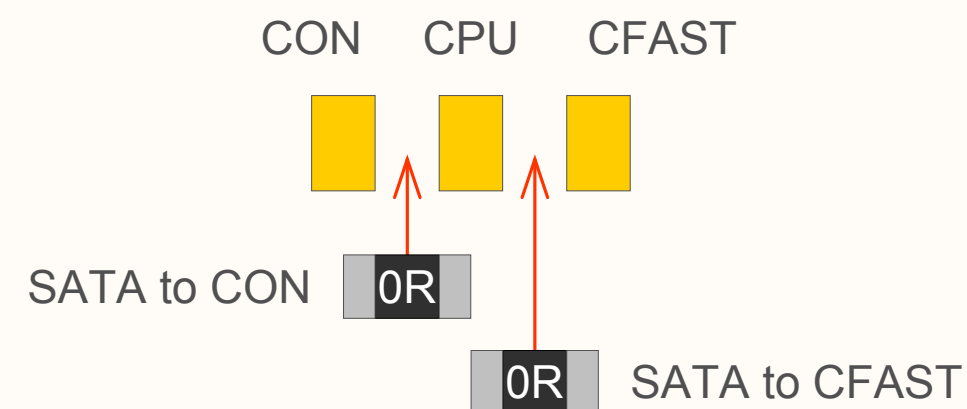
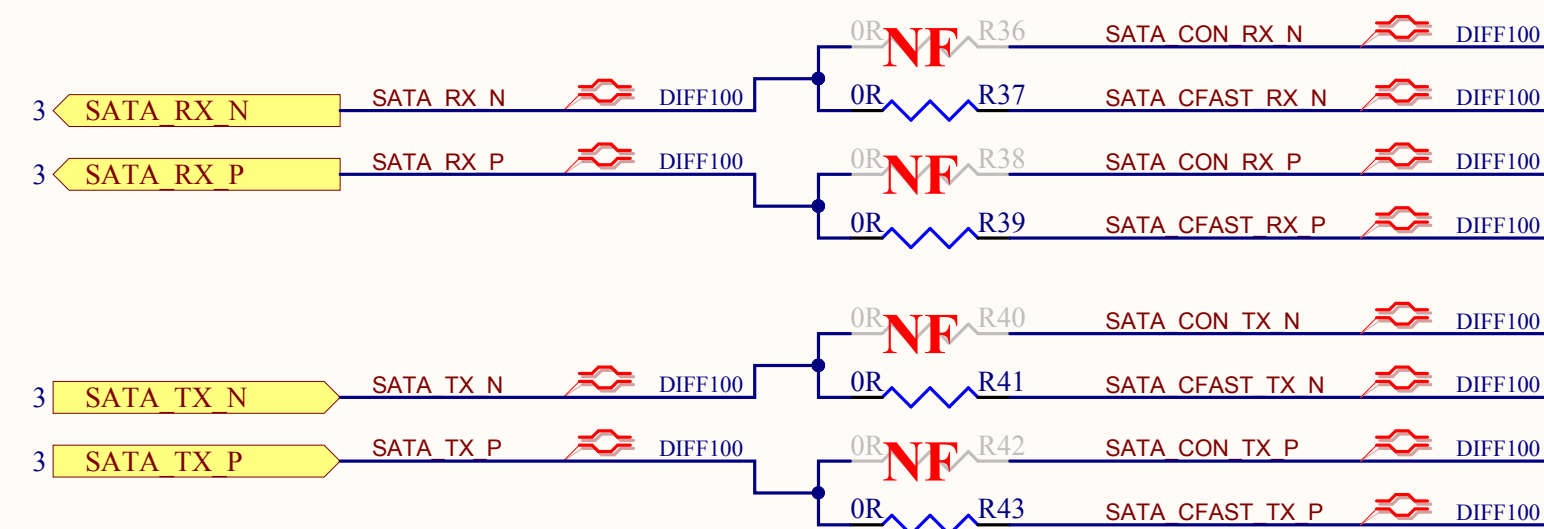
Speaker OUT



SATA, CFAST

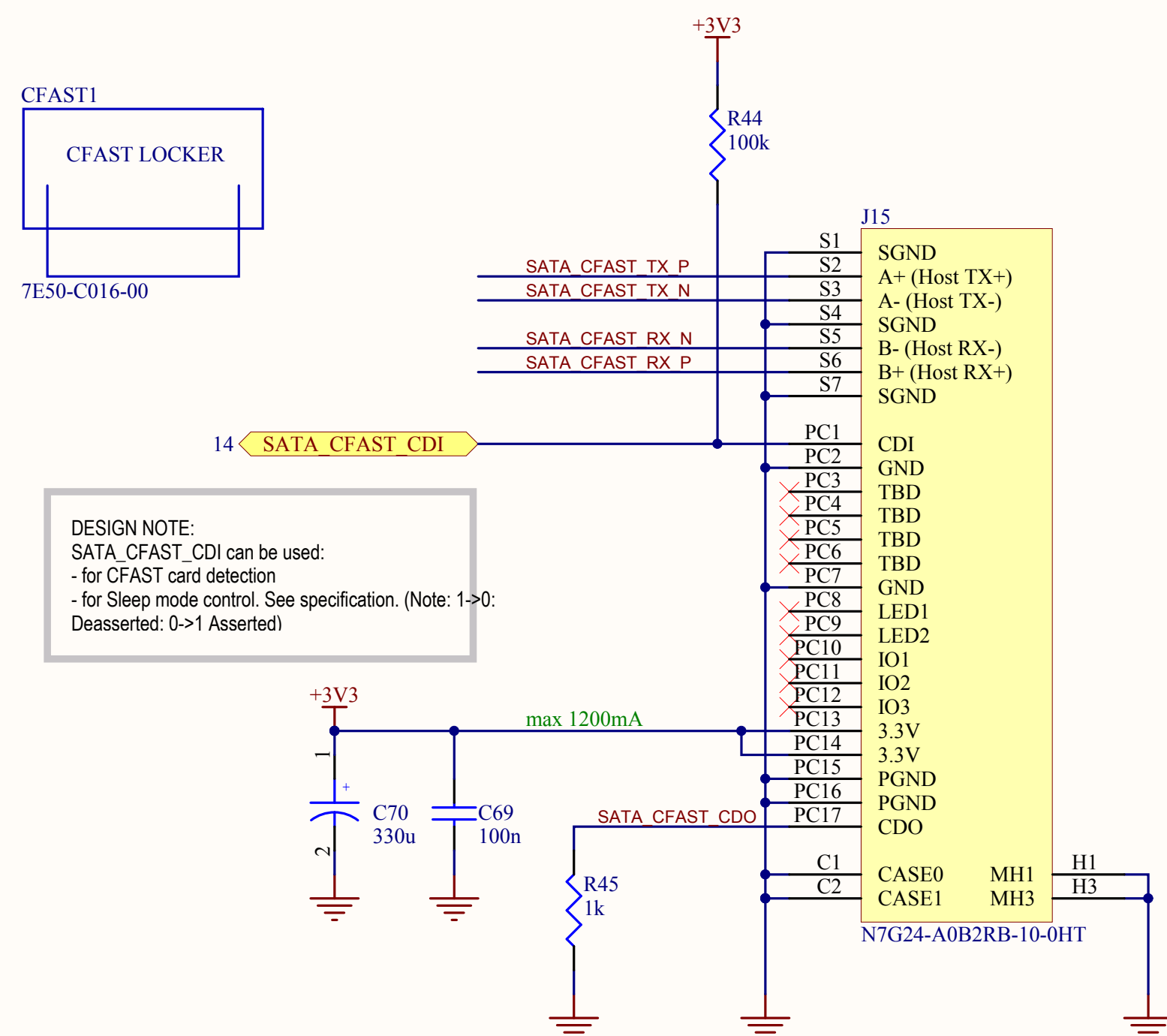
SATA Routing

DESIGN NOTE:
Fit only one resistor per signal according
to the picture below.

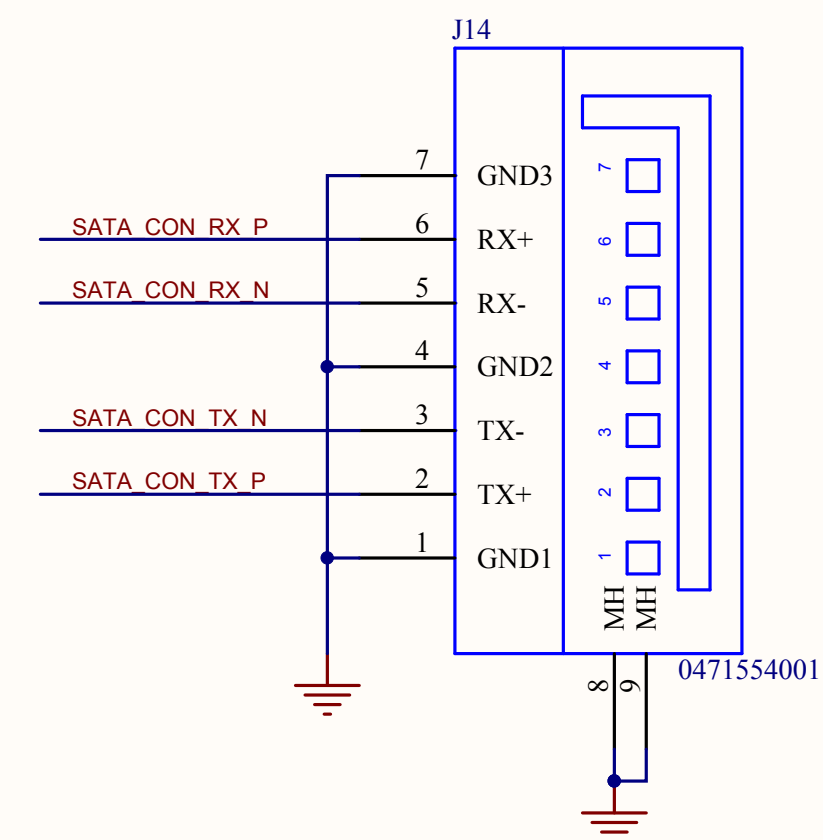


Net Class
ClassName: SATA

CFAST



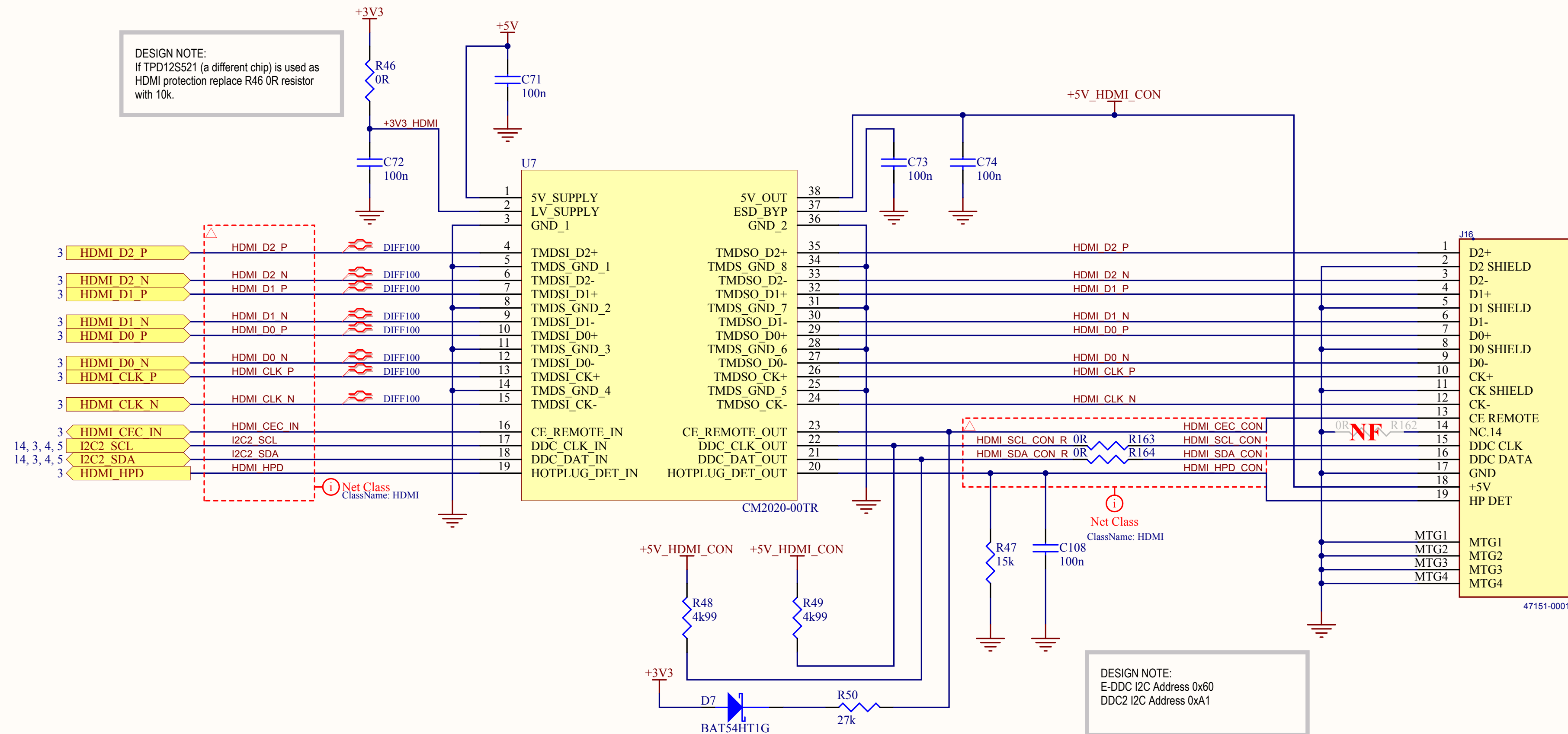
SATA



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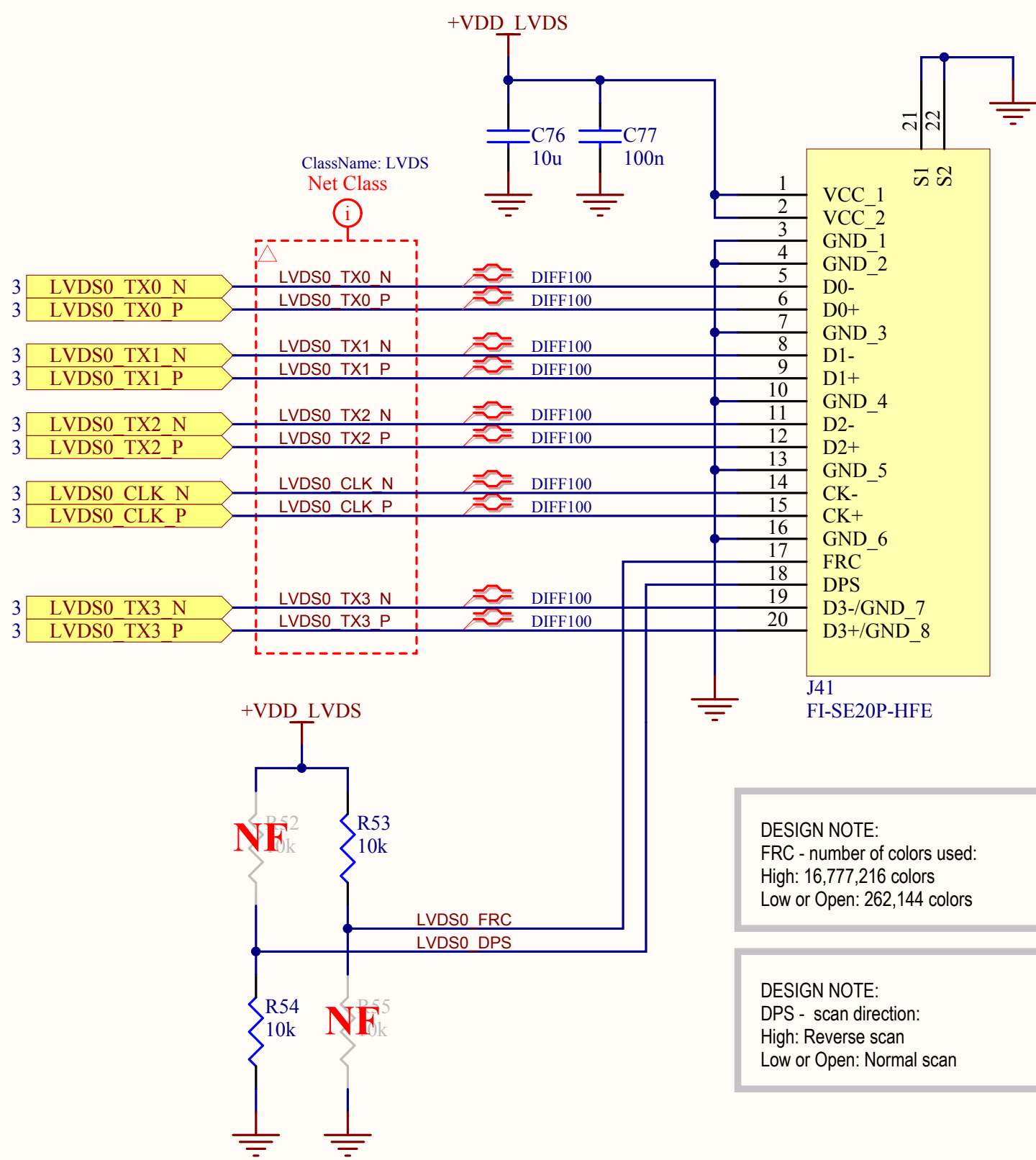
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Size:	DWG NO		Revision: VIII
Date:	12/3/2013		Sheet 6 of 20

HDMI



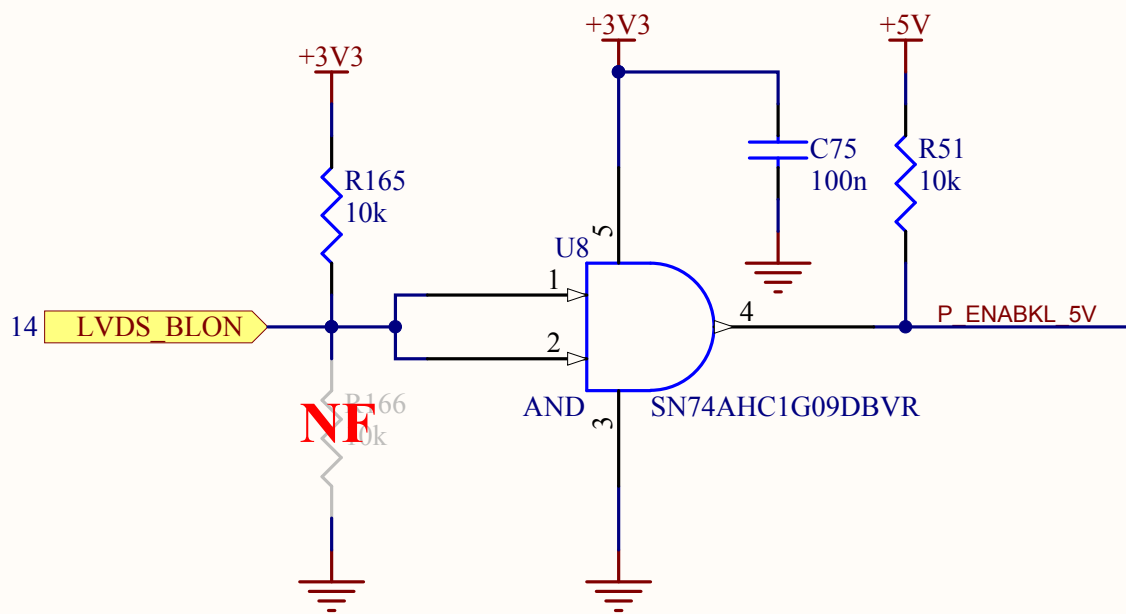
LVDS

LVDS Connector

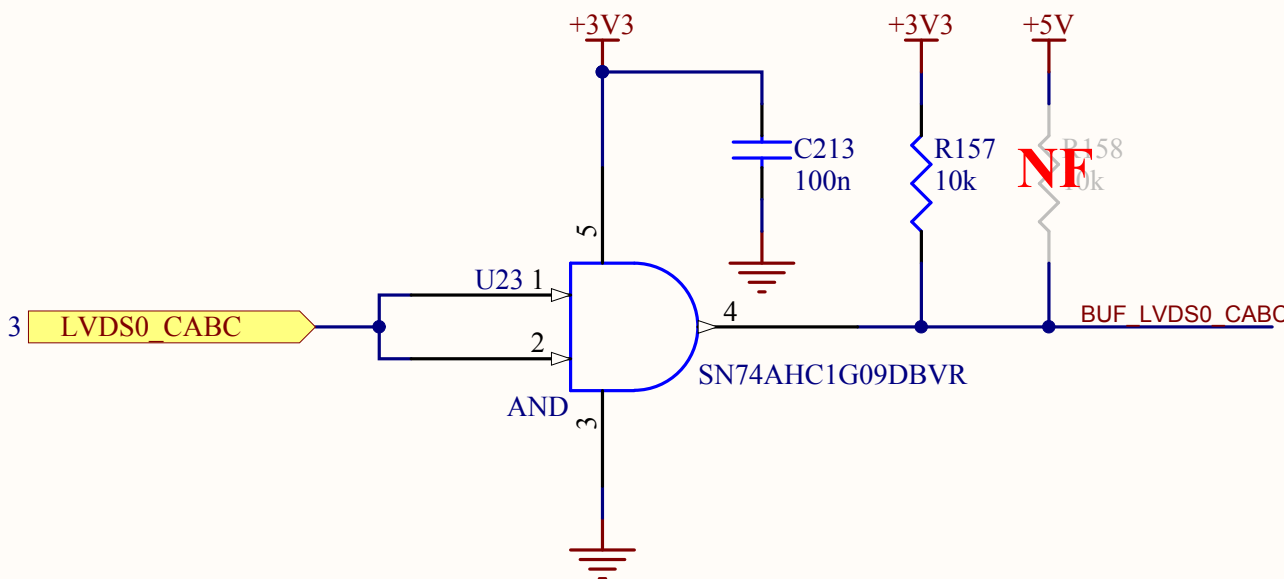


DESIGN NOTE:
Fit pullup to LVDS_BLOW for prototype only. Once a software support is implemented, pull the LVDS_BLOW to low by default.

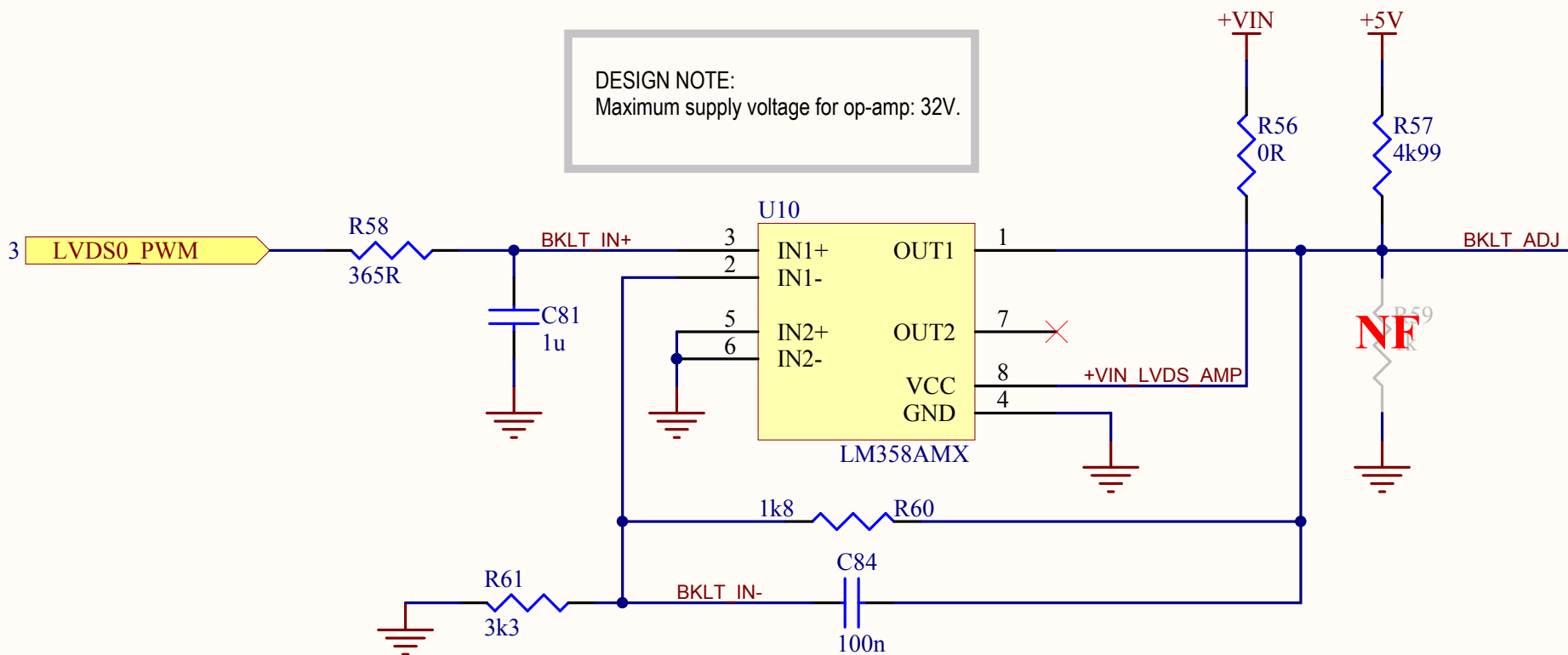
Display enable



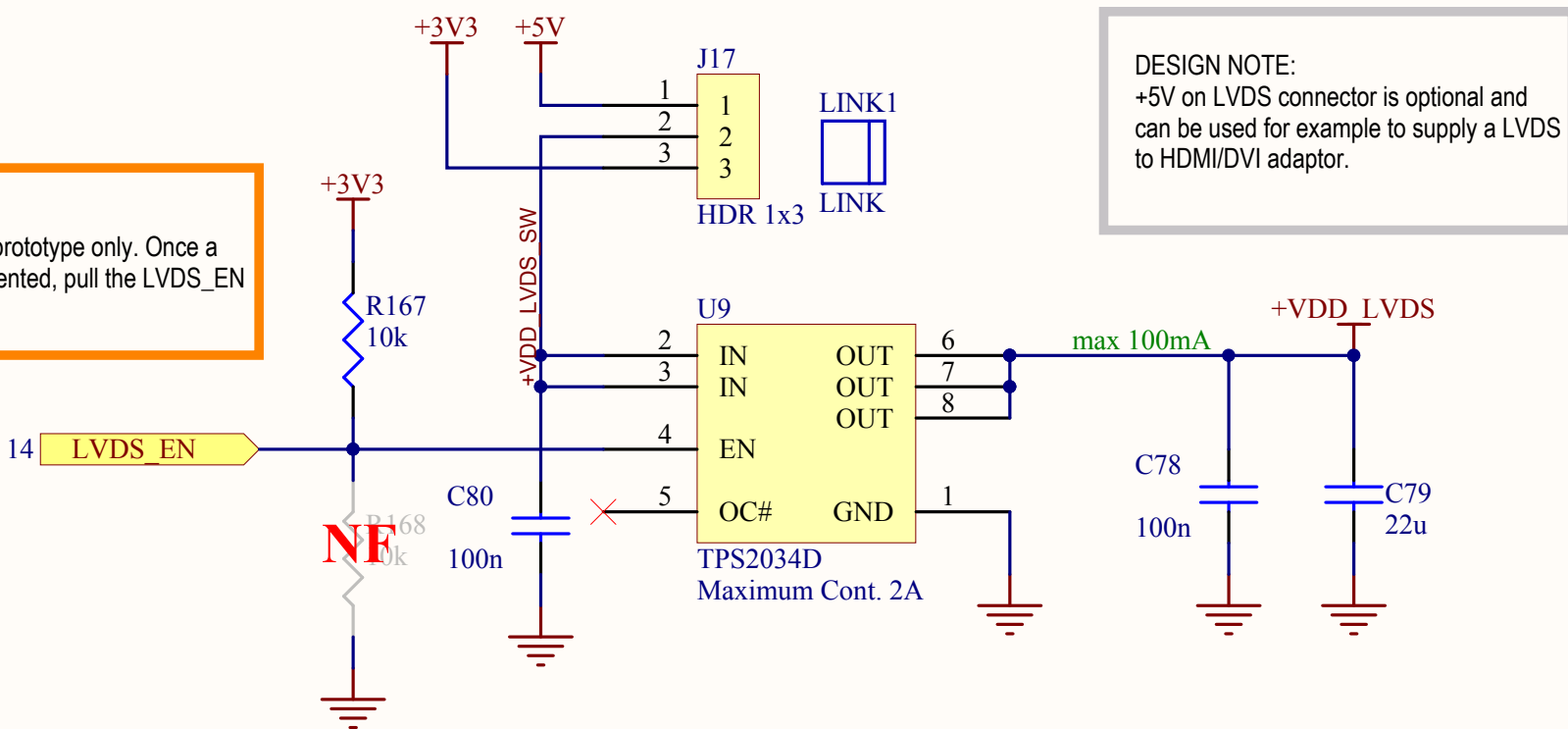
LVDS0 CABC buffer



Backlight adjustment

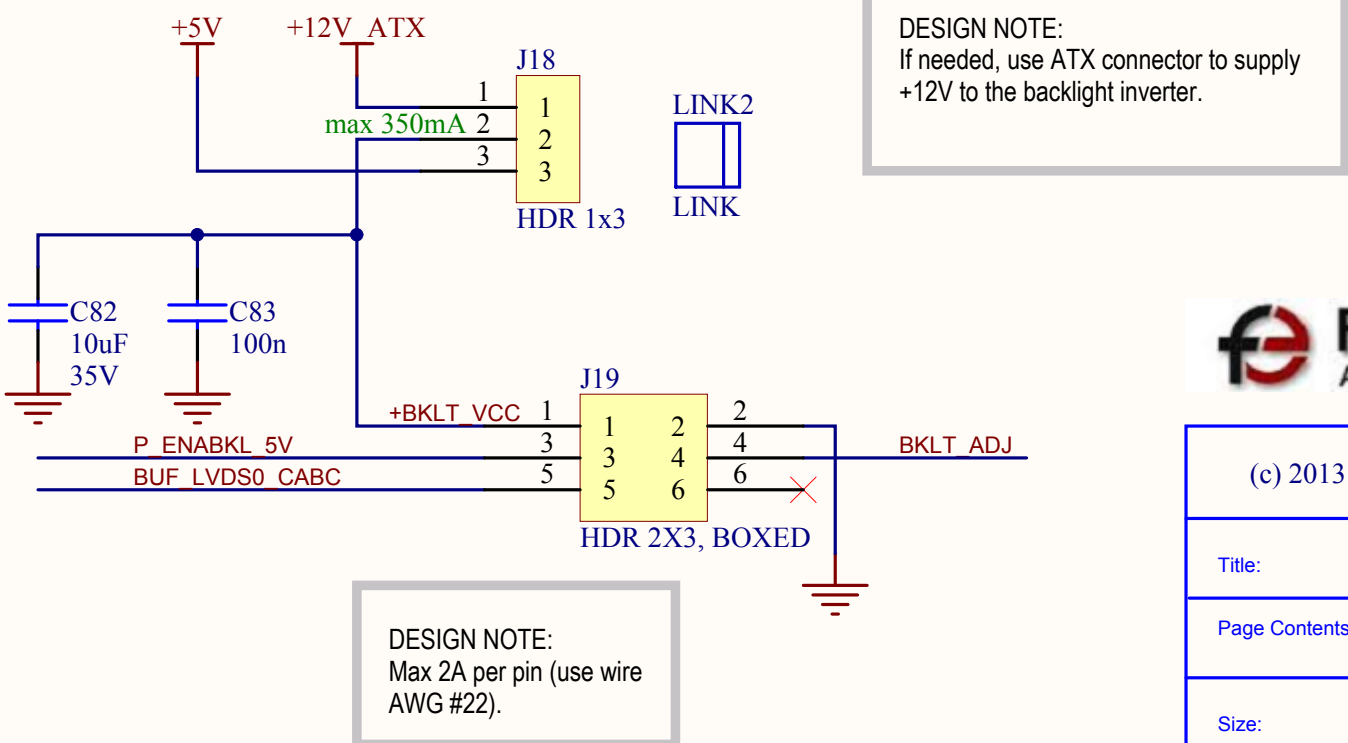


LVDS Switch



DESIGN NOTE:
Fit pullup to LVDS_EN for prototype only. Once a software support is implemented, pull the LVDS_EN to low by default.

Backlight connector

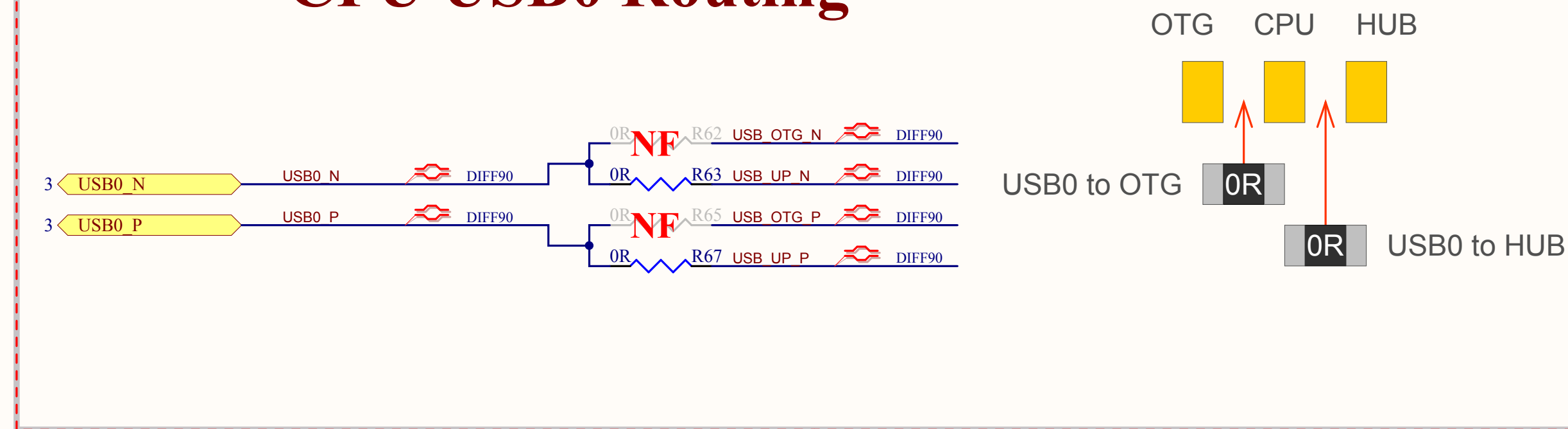


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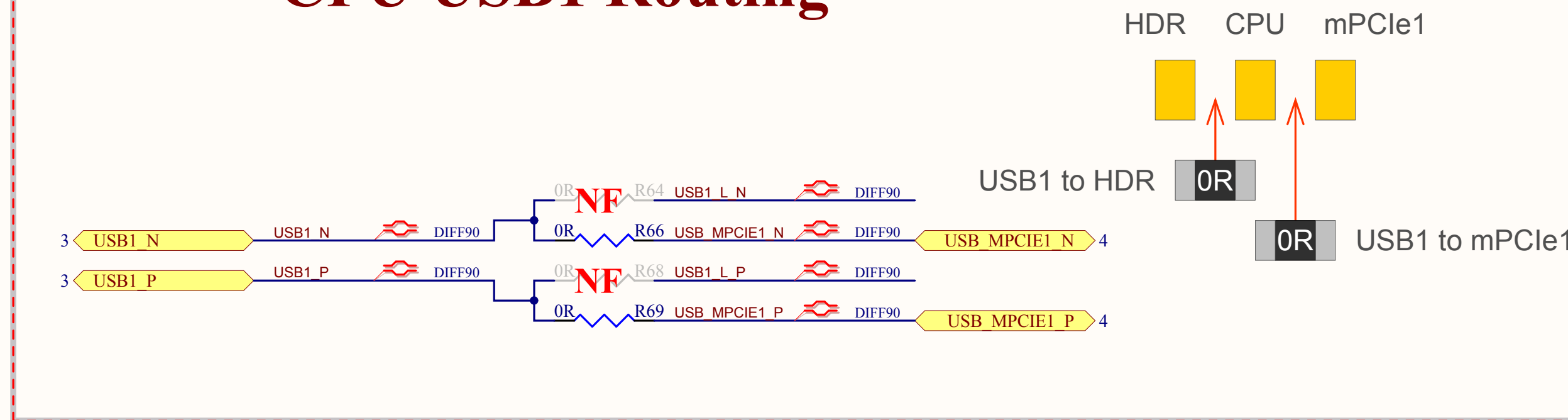
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Size:	DWG NO		Revision: V111
Date:	12/3/2013		Sheet 8 of 20

USB

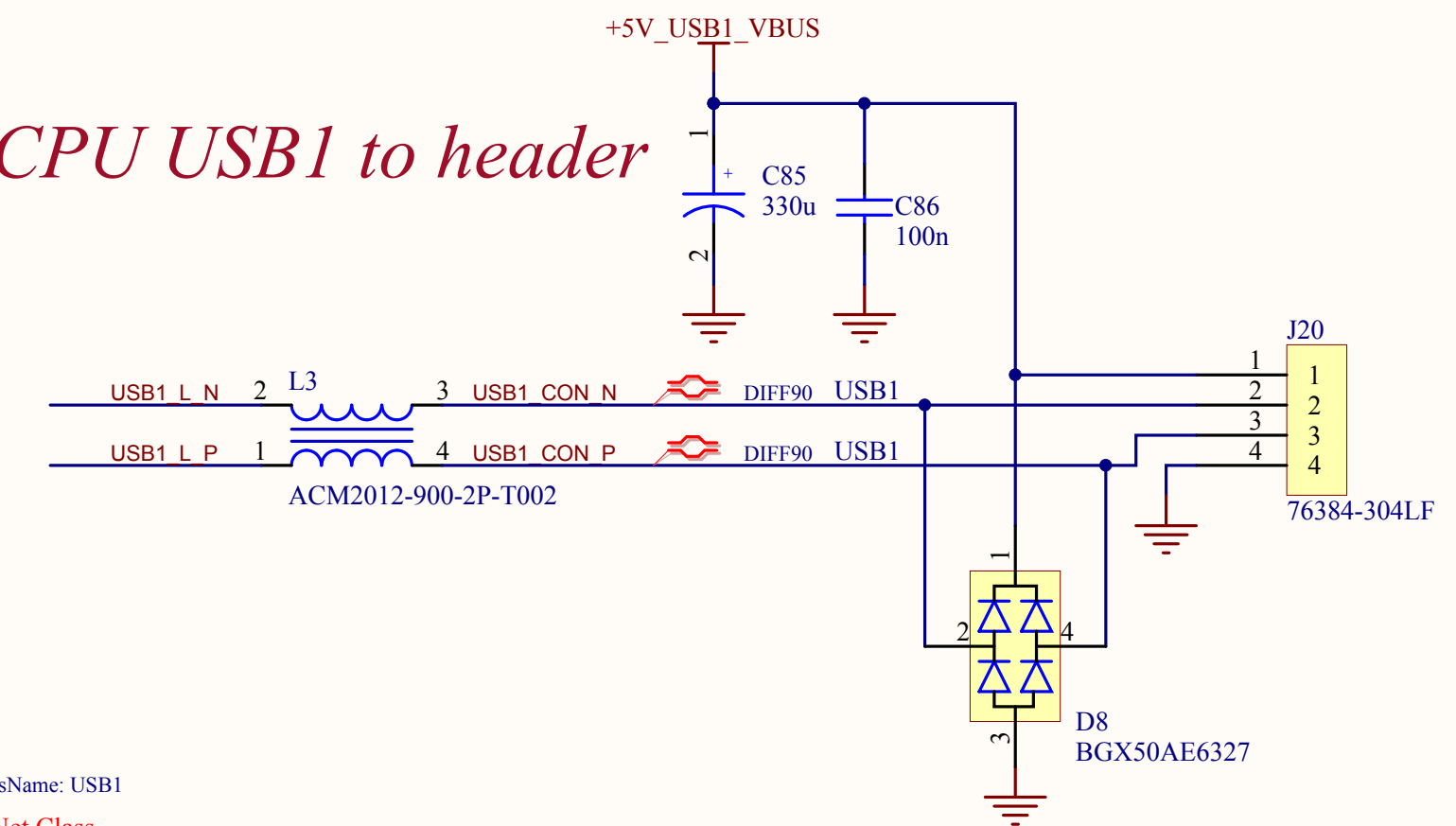
CPU USB0 Routing



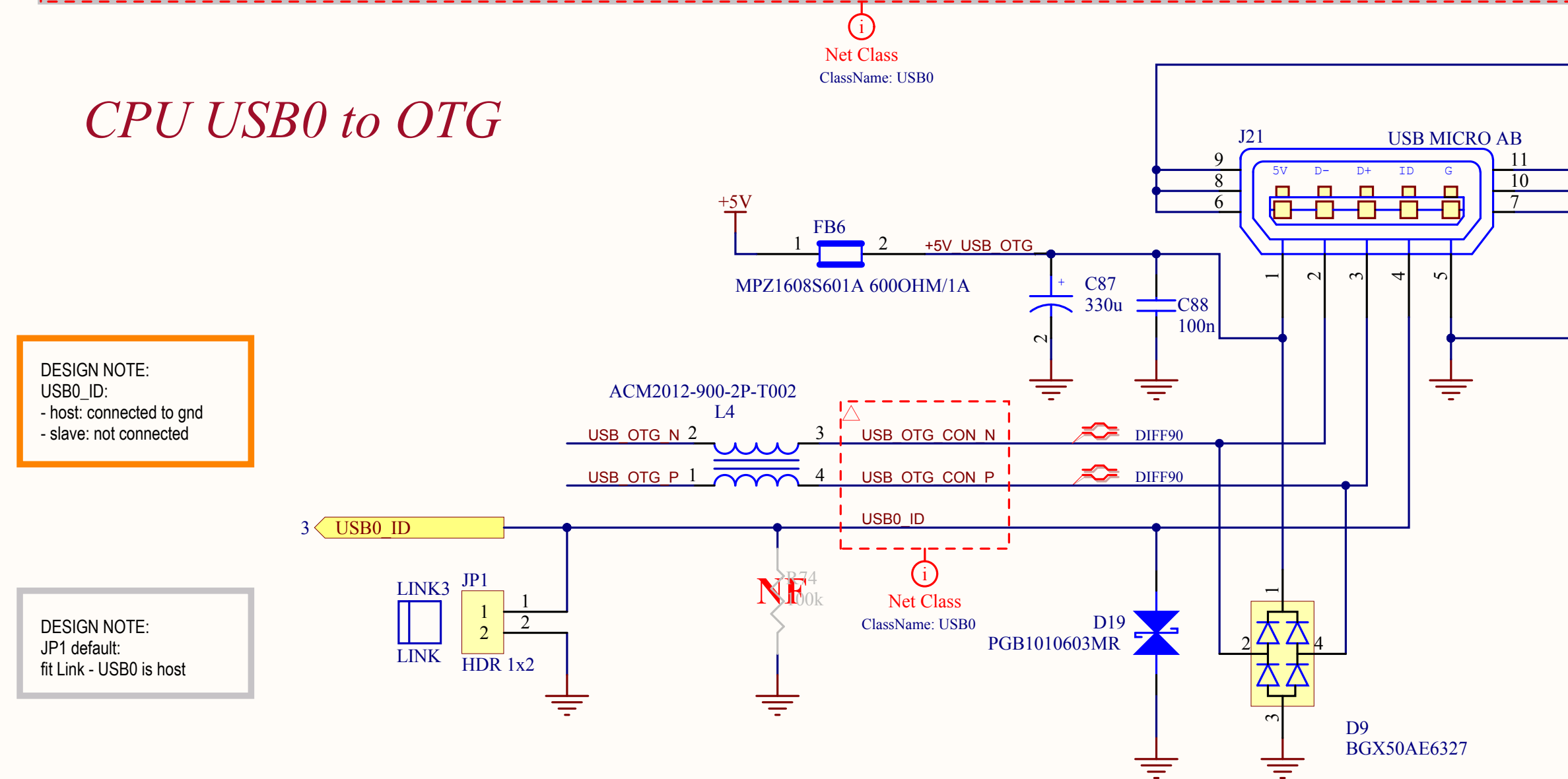
CPU USB1 Routing



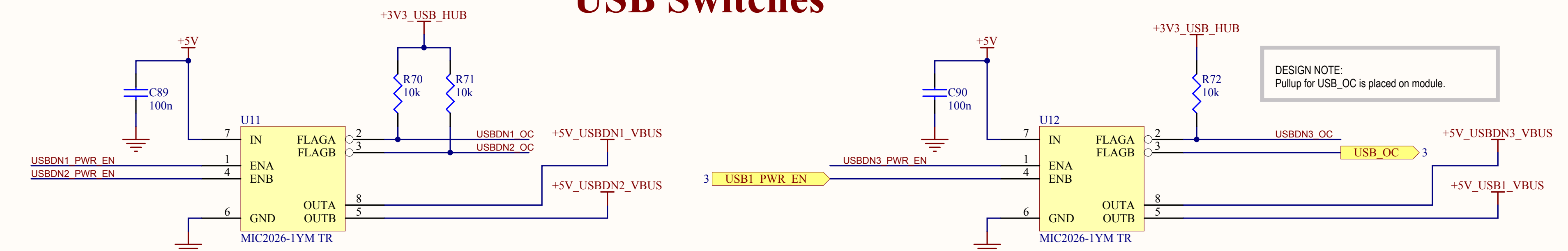
CPU USB1 to header



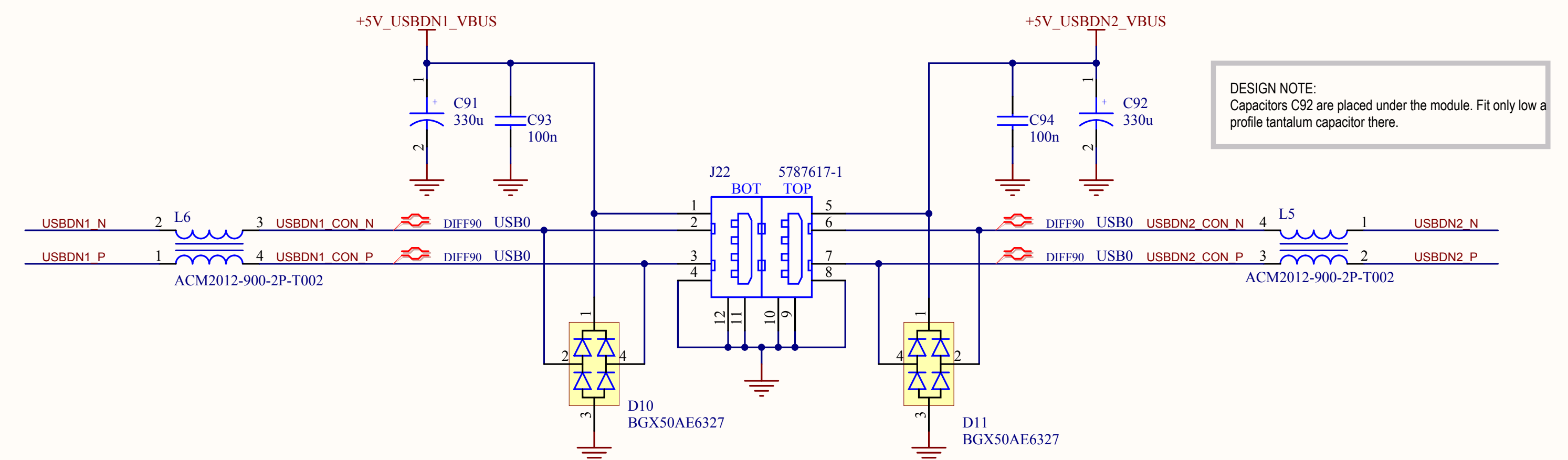
CPU USB0 to OTG



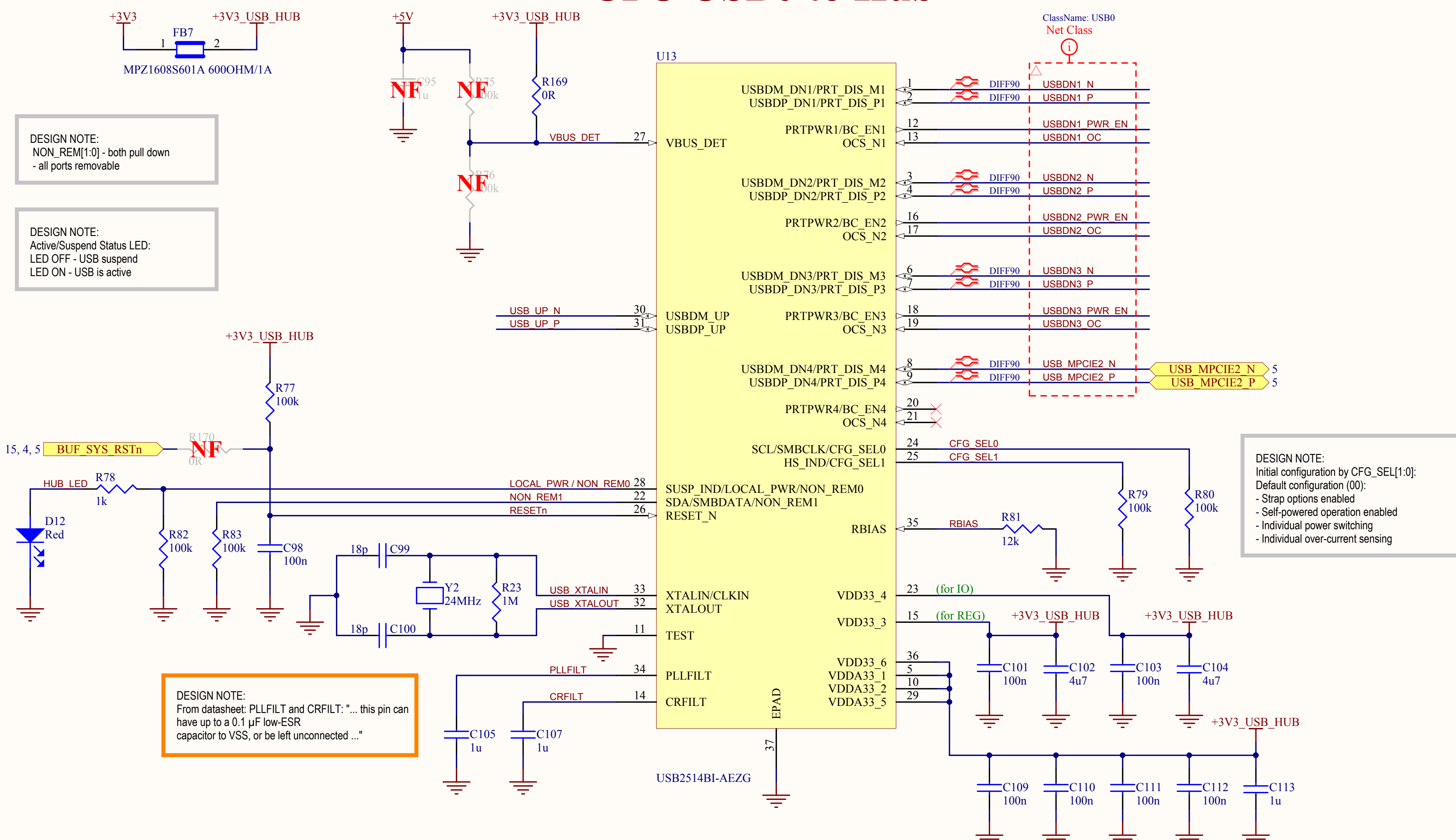
USB Switches



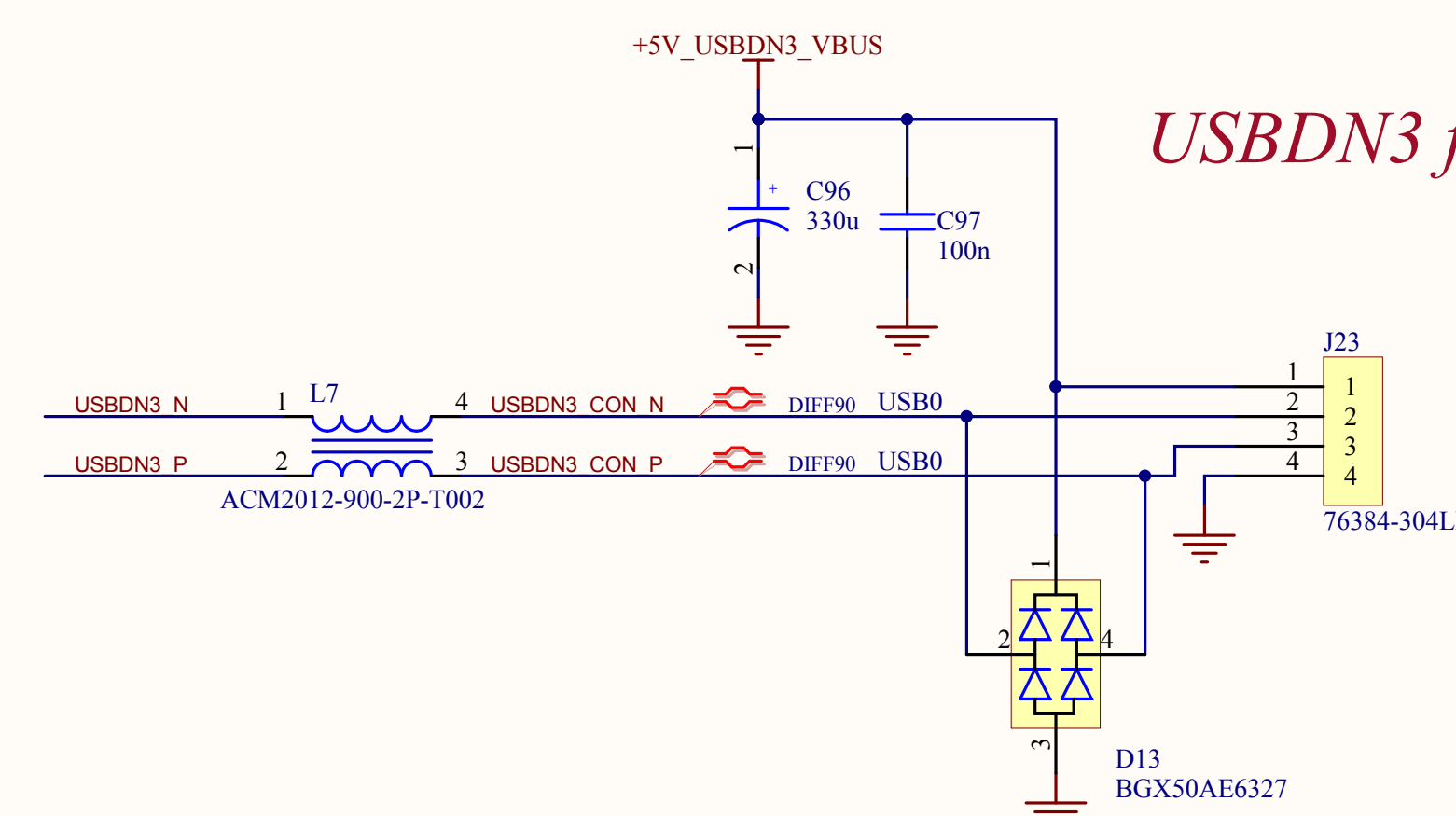
USBDN1 & USBDN2 from HUB



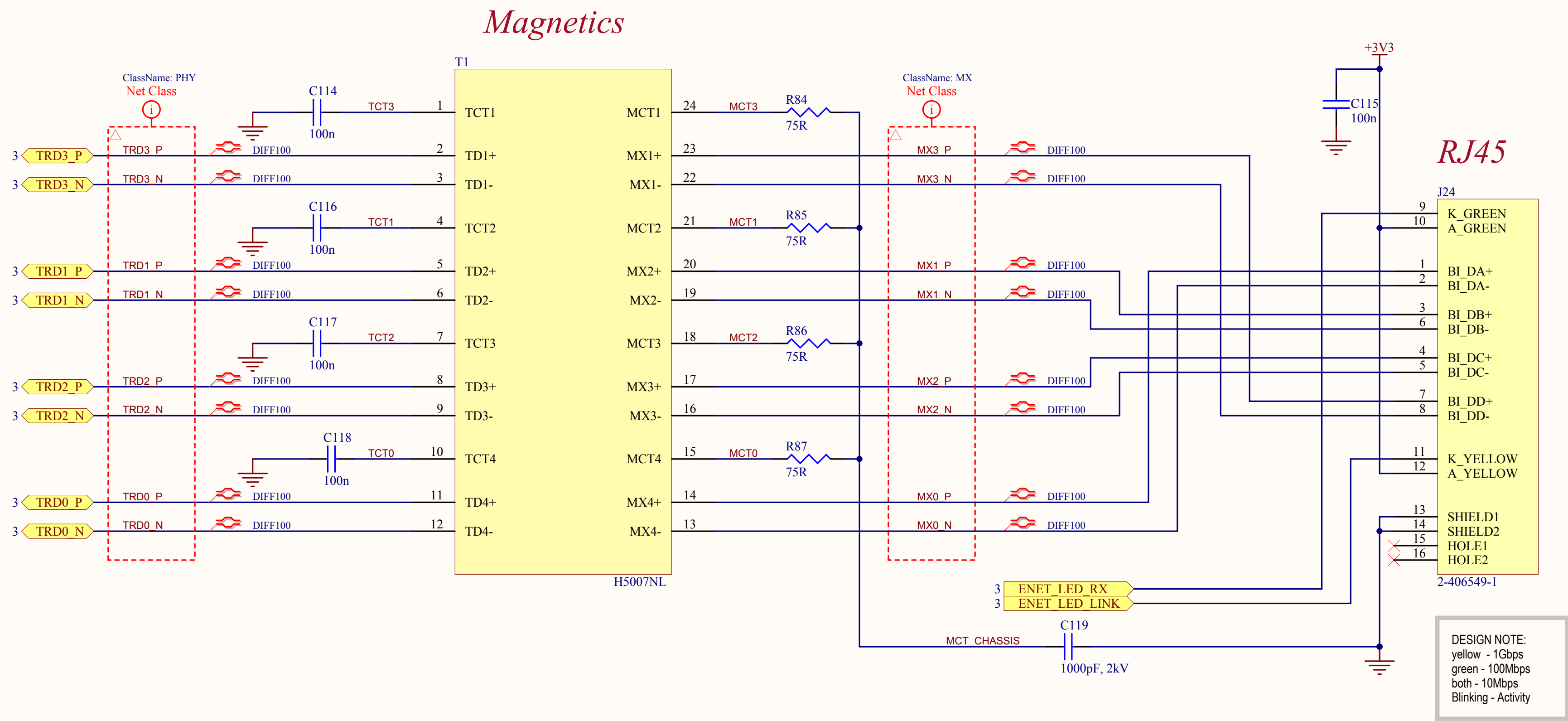
CPU USB0 to Hub



USBDN3 from HUB



ETHERNET



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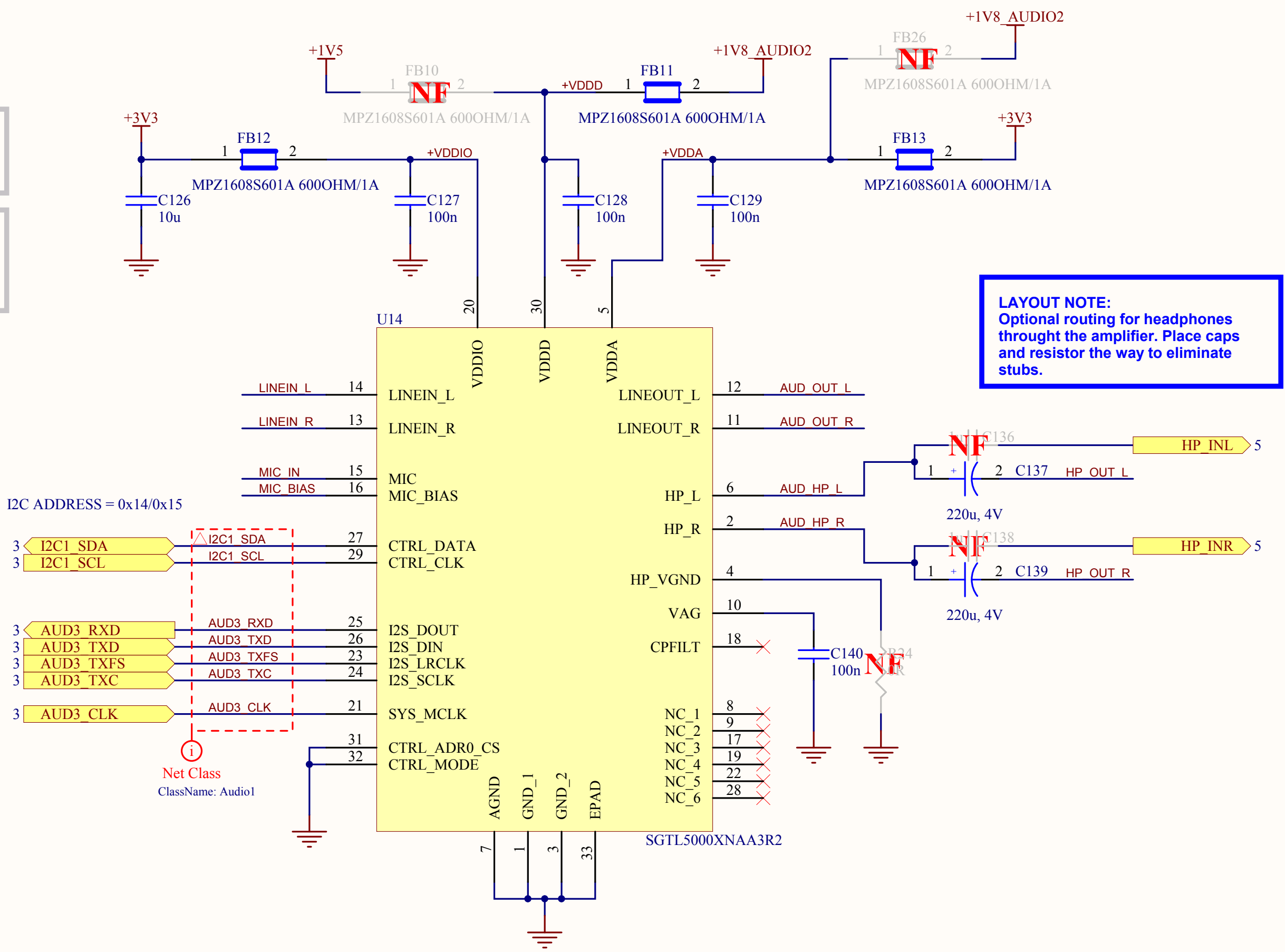
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Size:	DWG NO		Revision: V111
Date:	12/3/2013		Sheet 10 of 20

AUDIO1

AUDIO CODEC
(System audio connected to CPU)

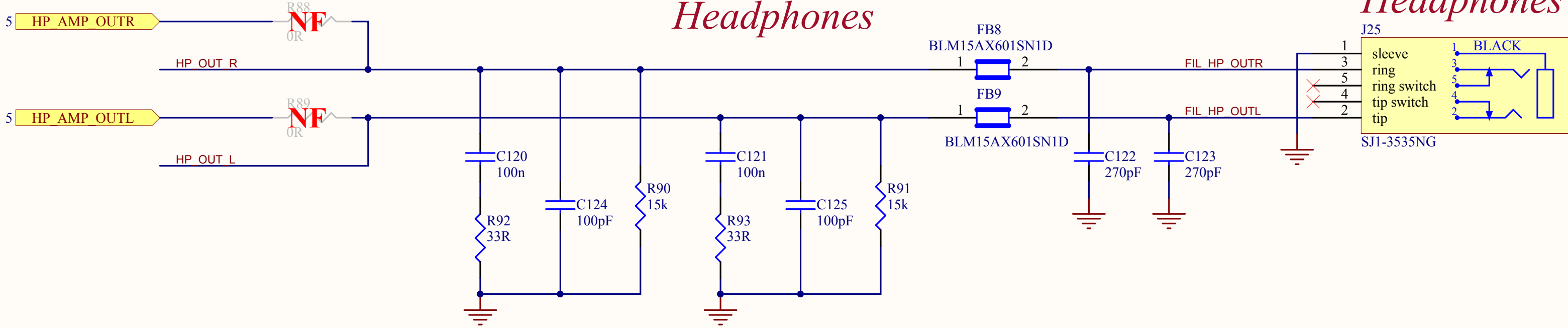
DESIGN NOTE:
External VDDO is required.

DESIGN NOTE:
If either VDDIO or VDDA is above 3V, the CPFILT pin must not be connected to capacitor.



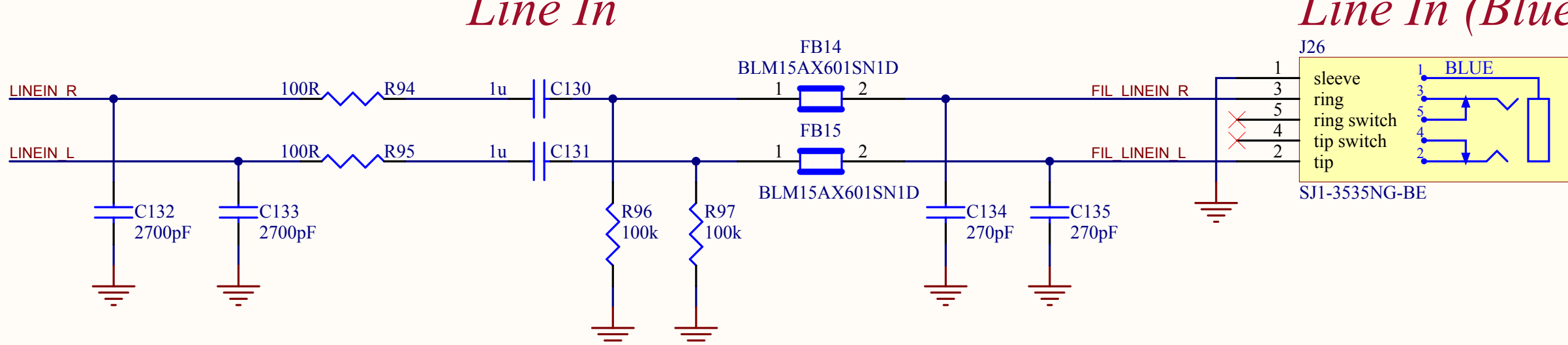
LAYOUT NOTE:
Optional routing for headphones through the amplifier. Place caps and resistor the way to eliminate stubs.

Headphones



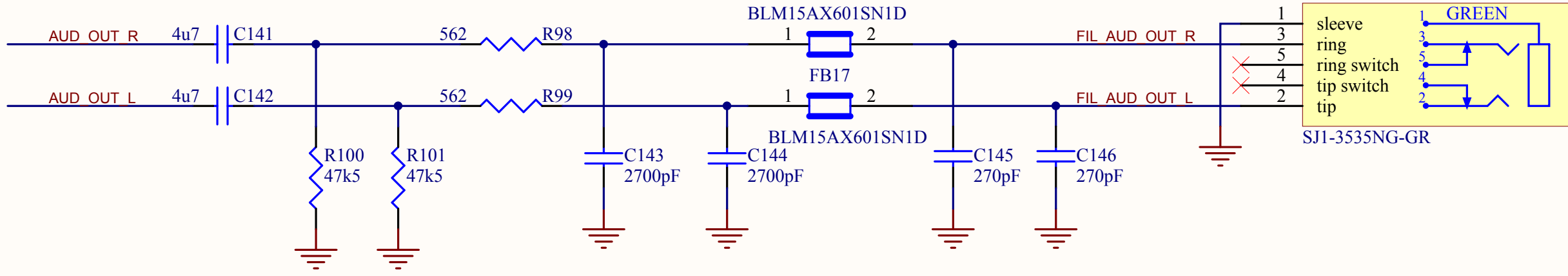
Headphones (Black)

Line In



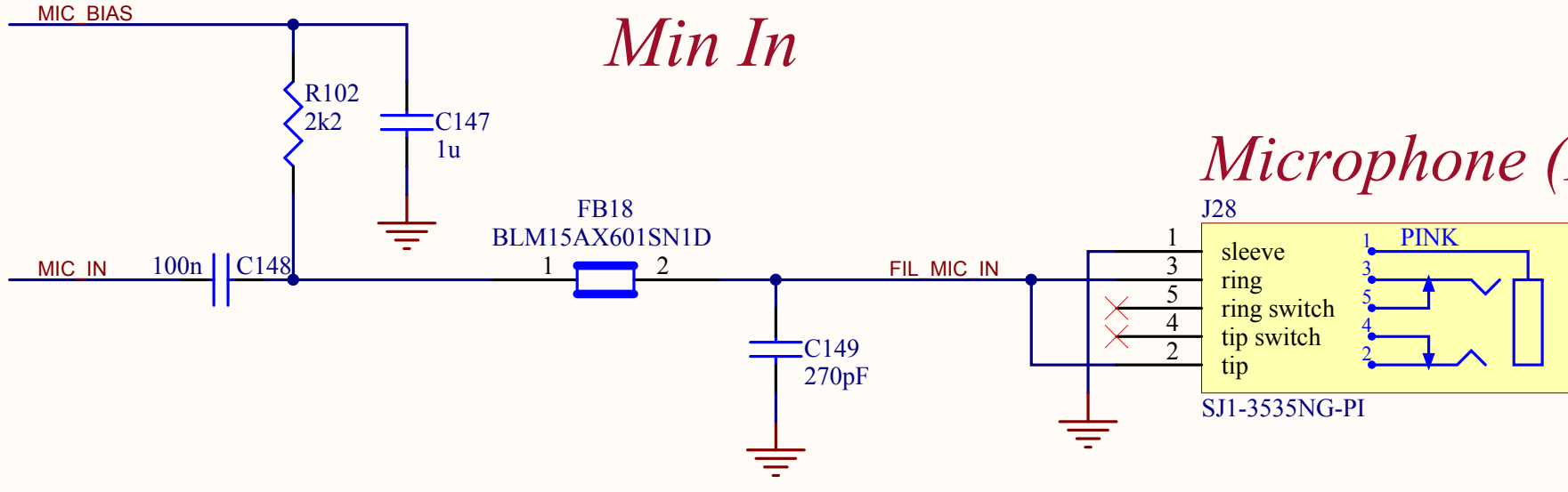
Line In (Blue)

Line Out



Line Out (Green)

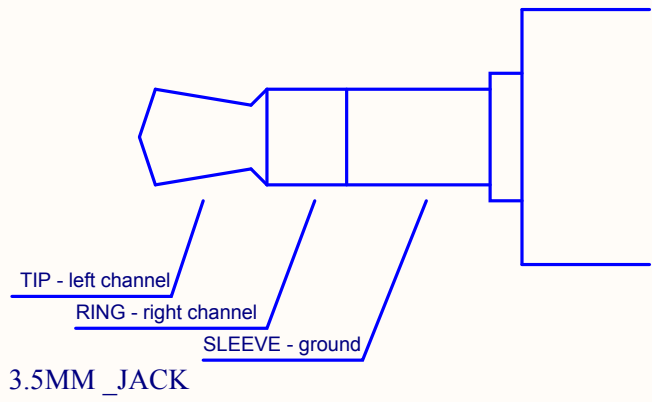
Min In



Microphone (Pink)

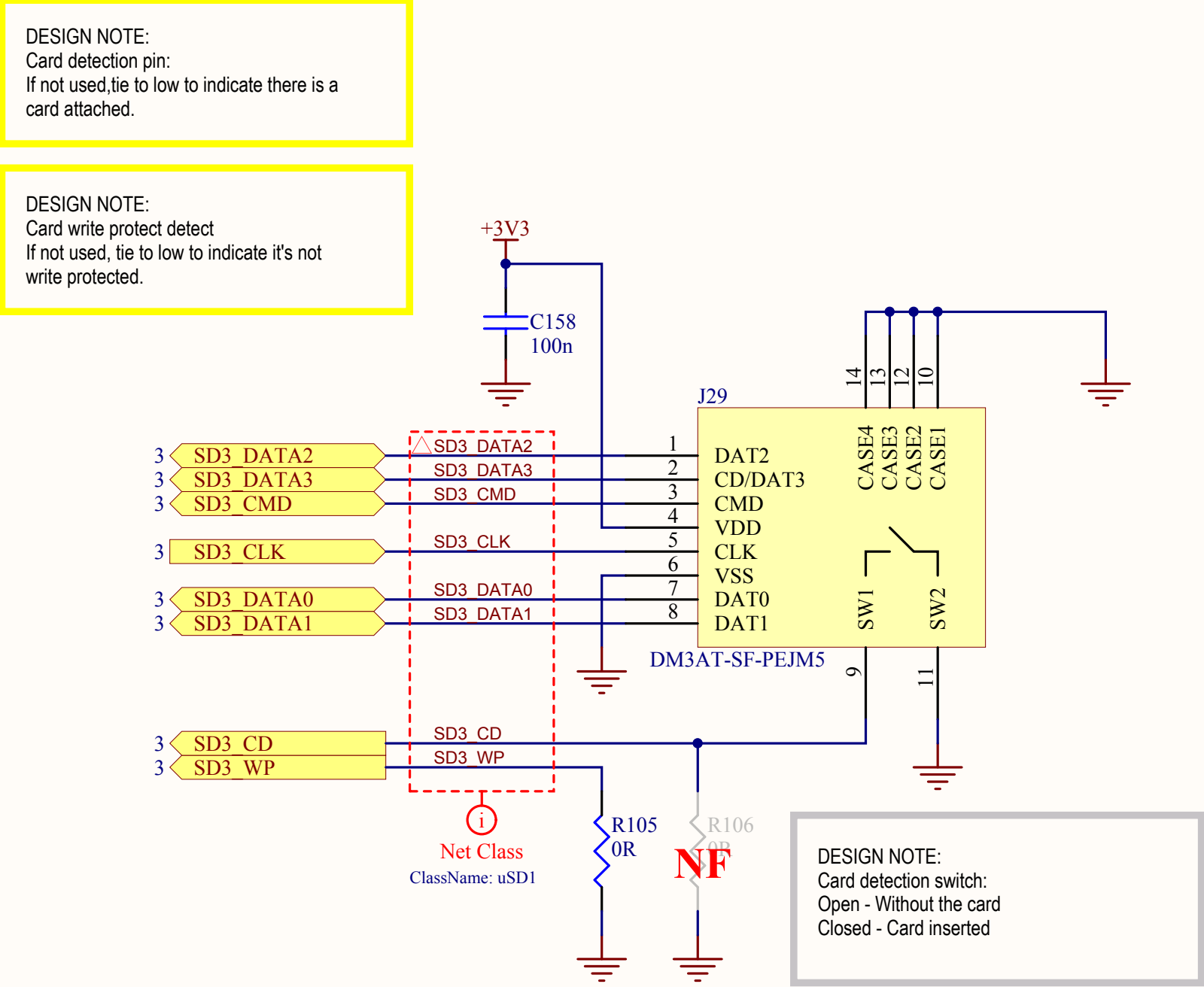
DESIGN NOTE:
Source for the audio filters is
http://www.cirrus.com/en/pubs/rd/Datasheet/CDB4207_DB1.pdf

3.5mm jack reference



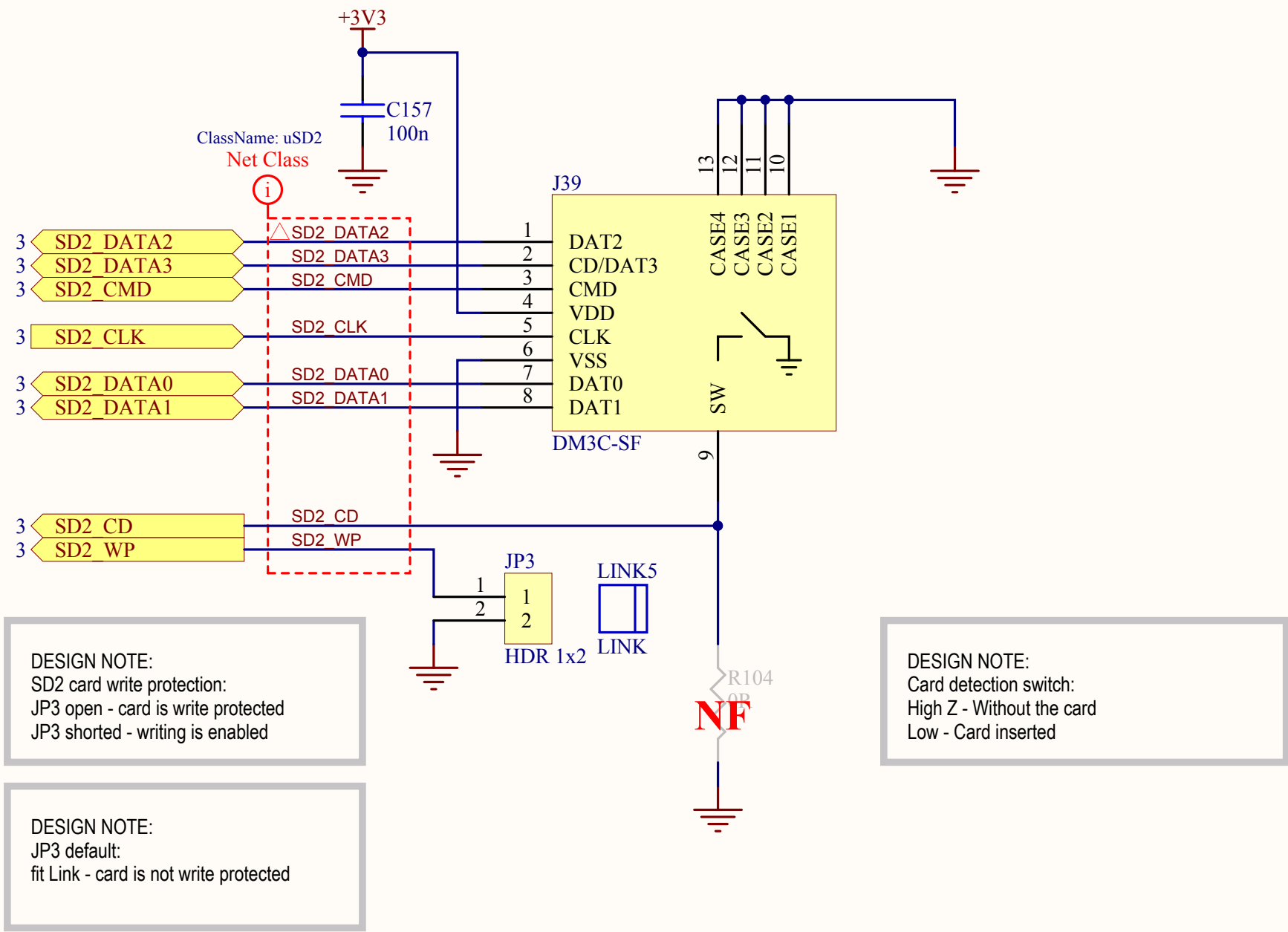
SD CARDS

Micro SD1

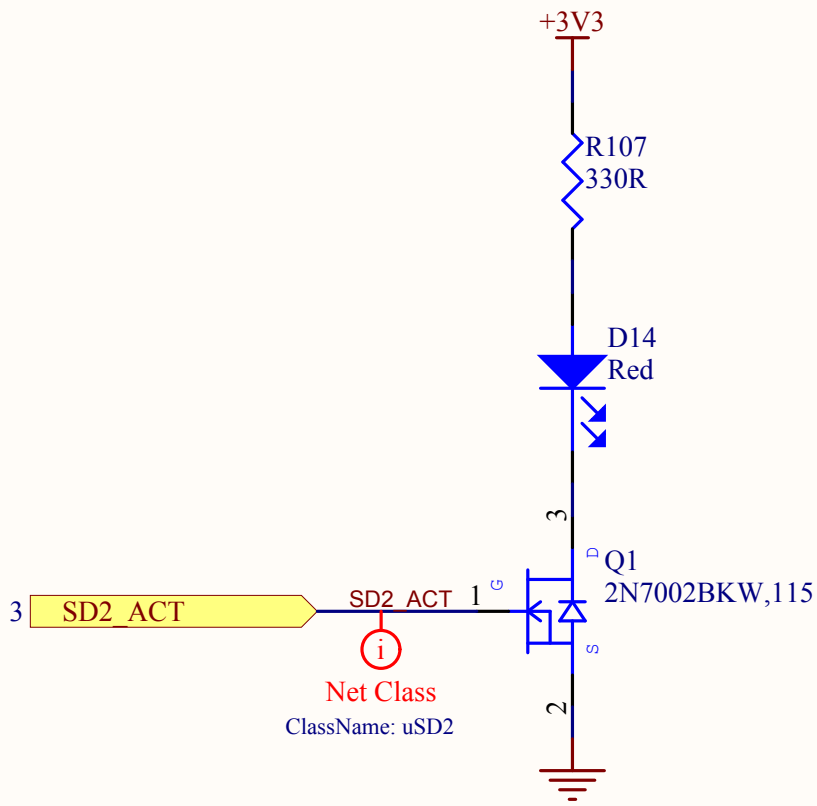


Micro SD2

(intended to use for OS storage)



uSD2 Activity LED

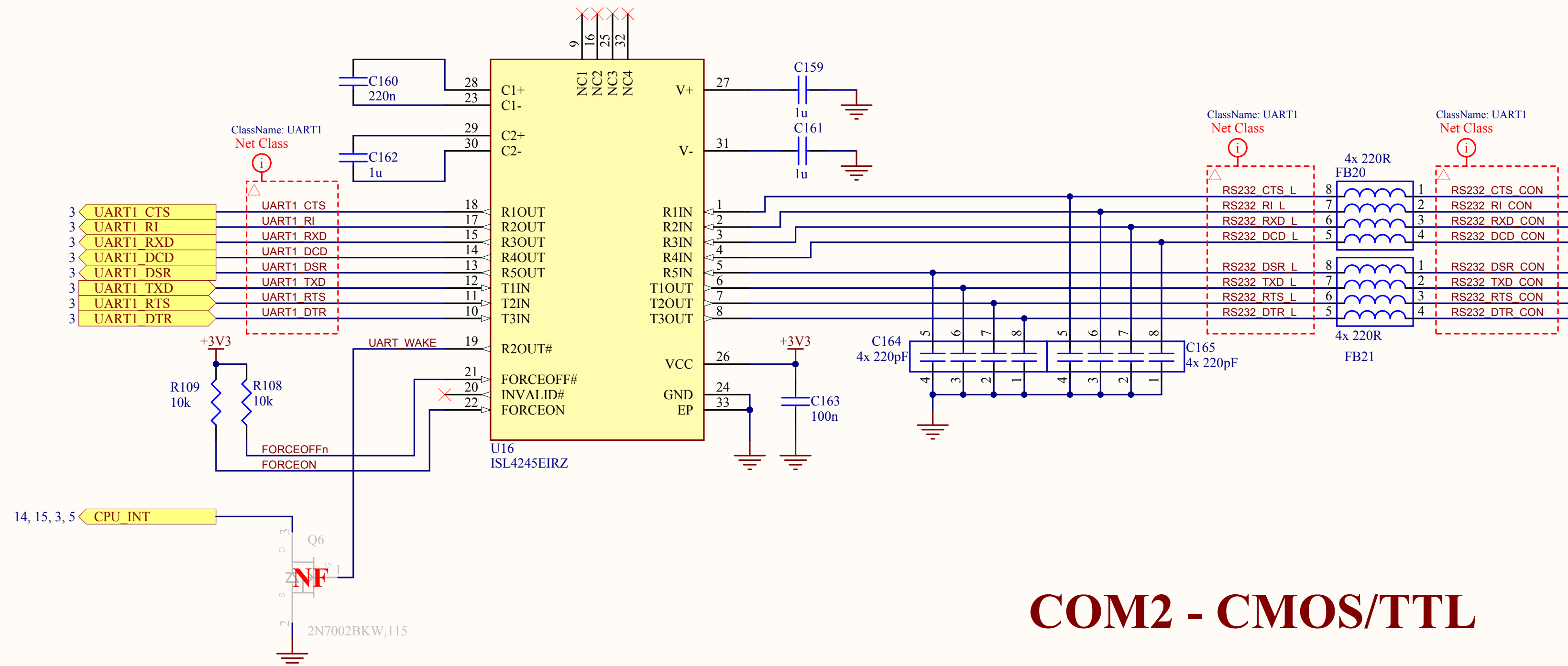


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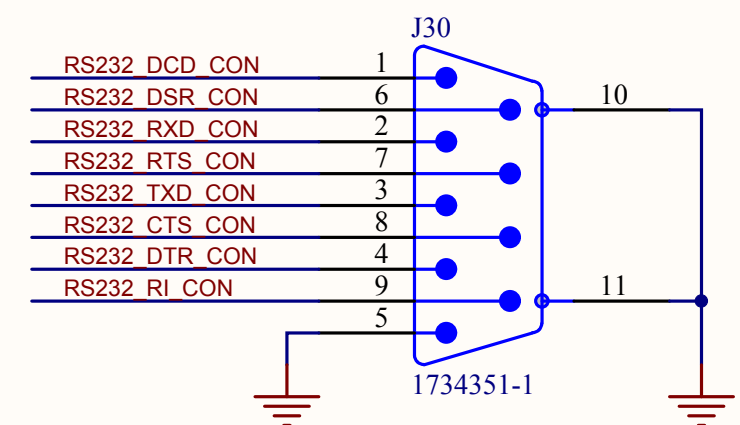
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Page Contents:	[12] - SD.SchDoc		Checked by
Size:	DWG NO		Revision: V111
Date:	12/3/2013		Sheet 12 of 20

UARTS

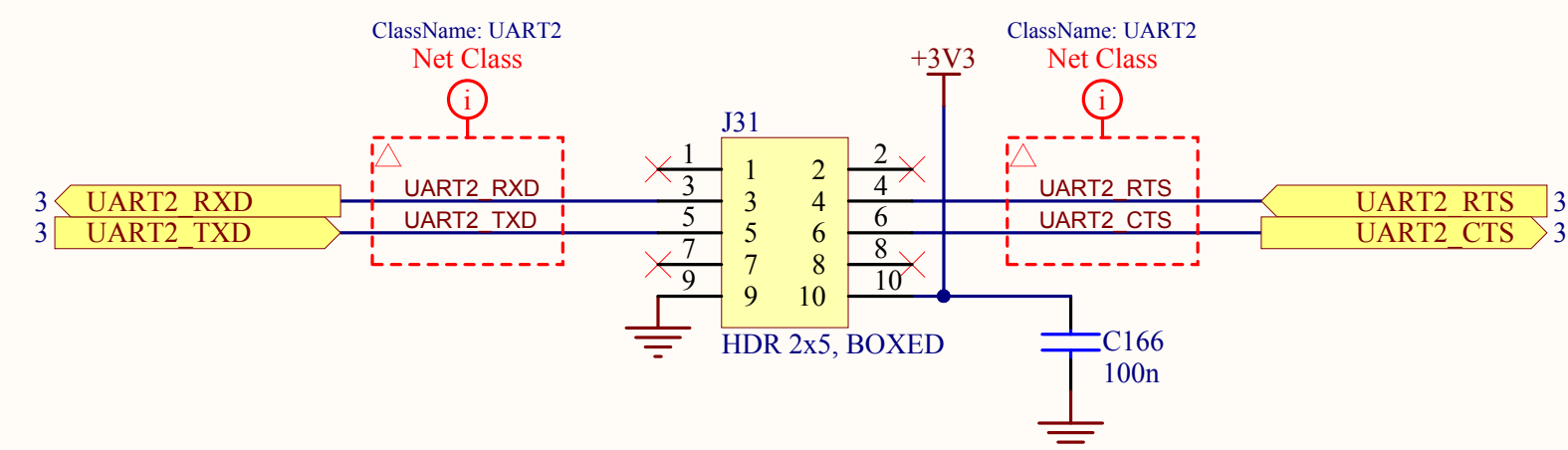
RS232 Transceiver



COM1 - RS232



COM2 - CMOS/TTL

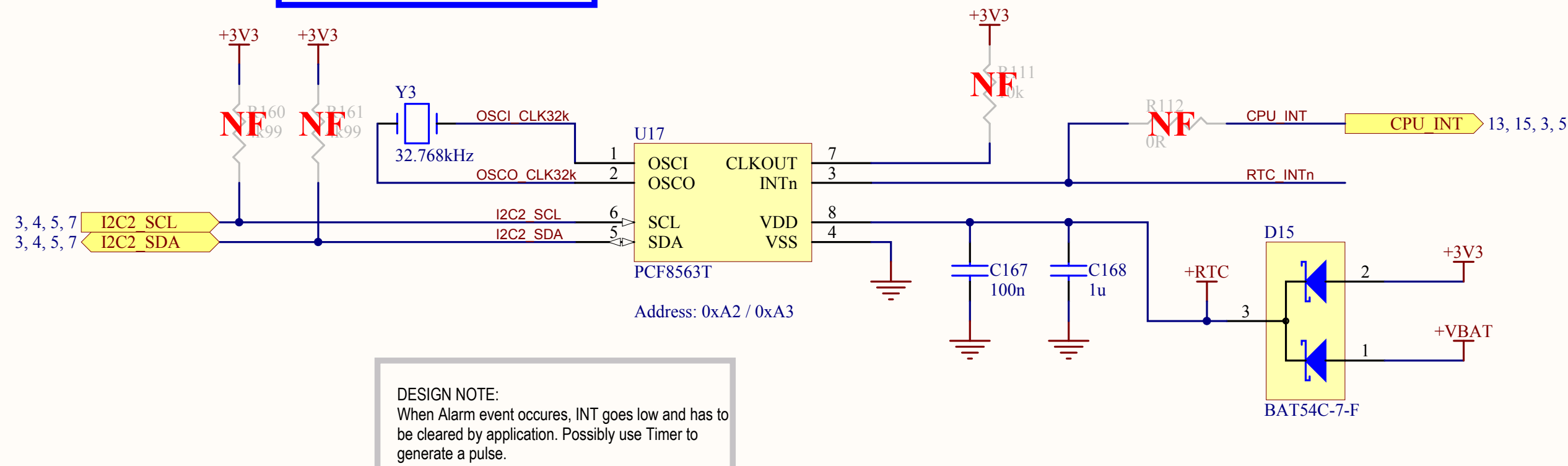


RTC, EEPROM, GPIO, TOUCH SCREEN

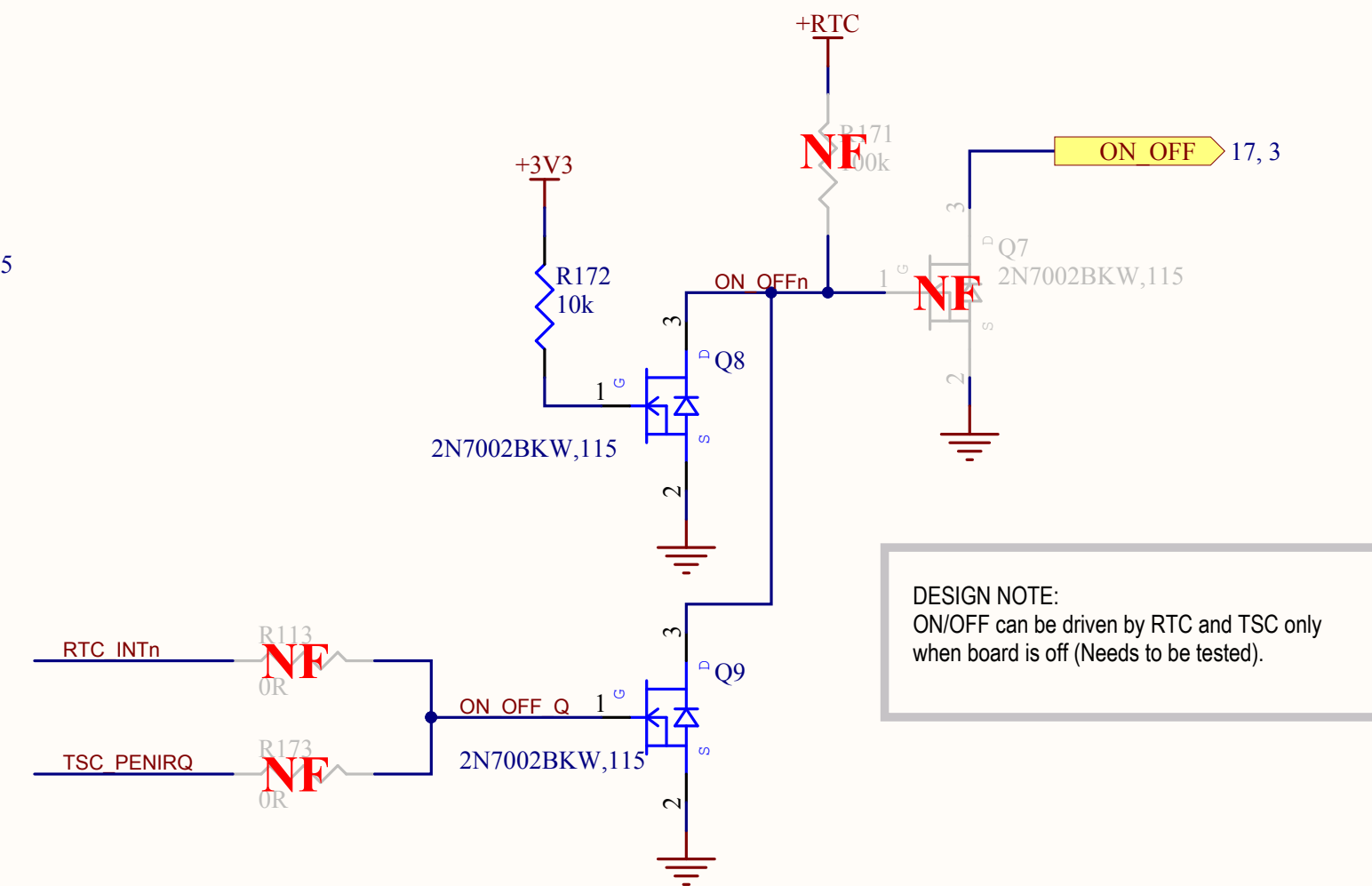
RTC Clock

DESIGN NOTE:
Fit optional pullups to I2C2 when there is a need for lower pullup value.

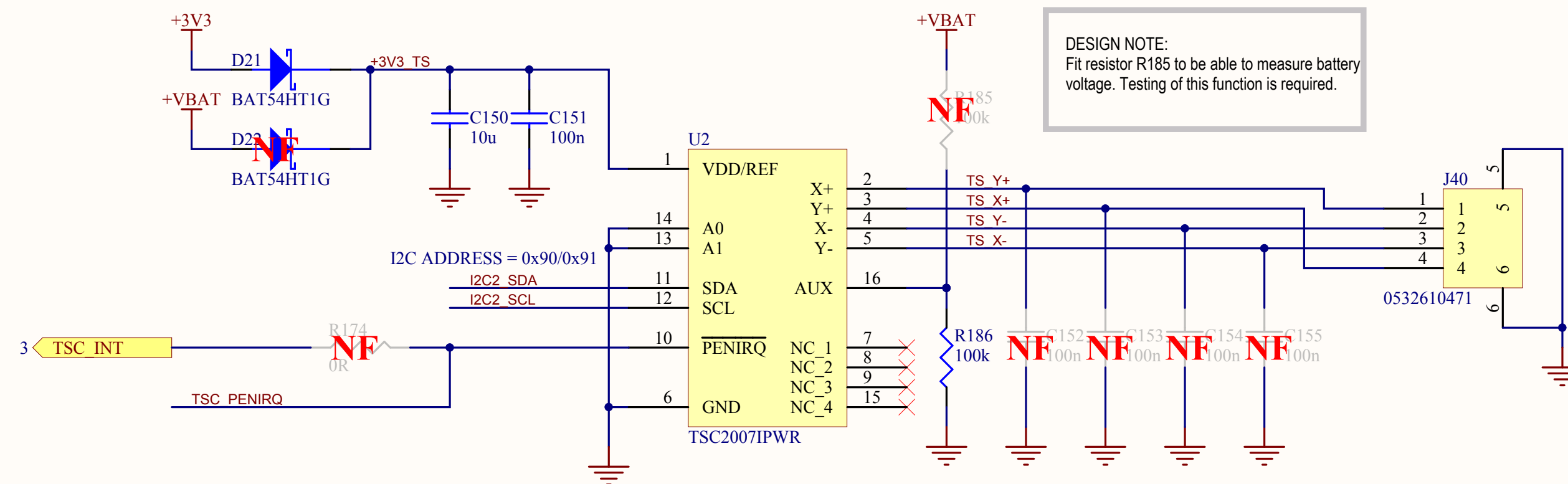
LAYOUT NOTE:
Place optional pullup resistor to the end of I2C lines.



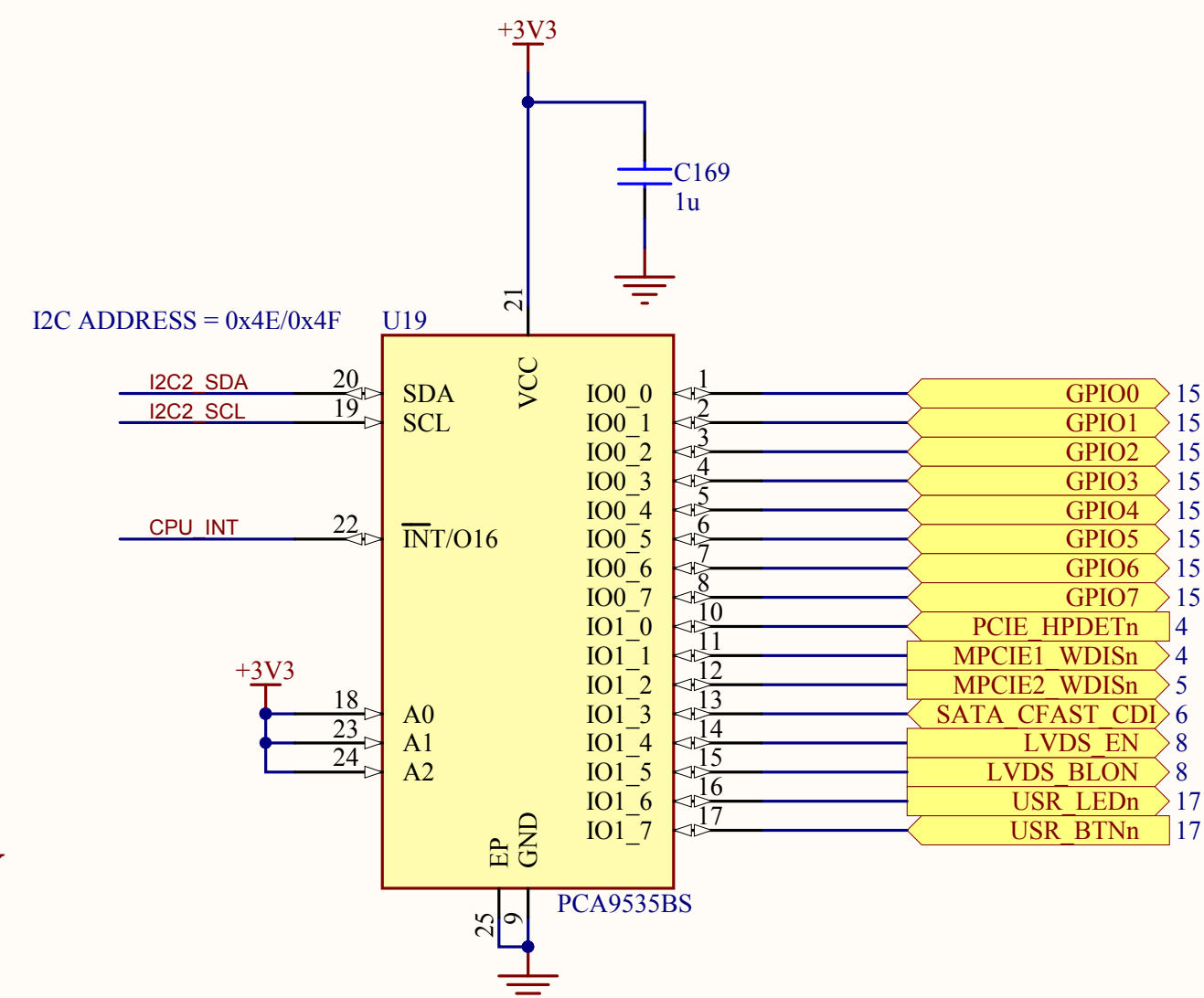
RTC & Touch screen ON/OFF support



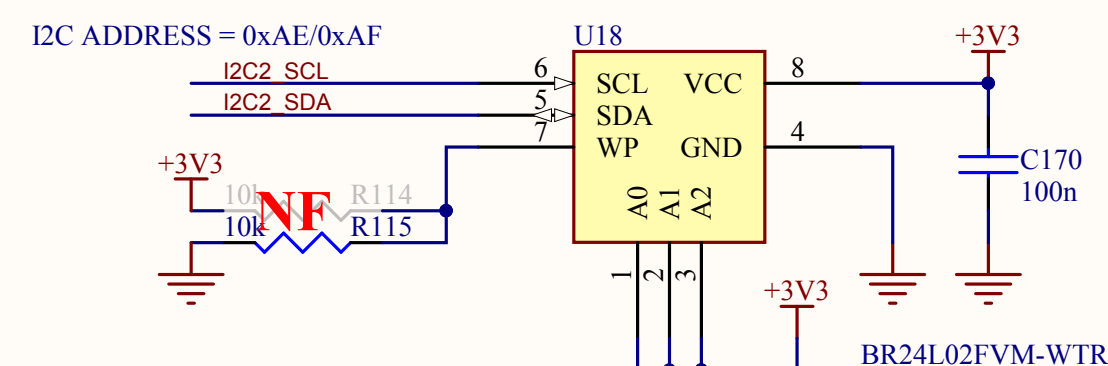
Touch screen controller



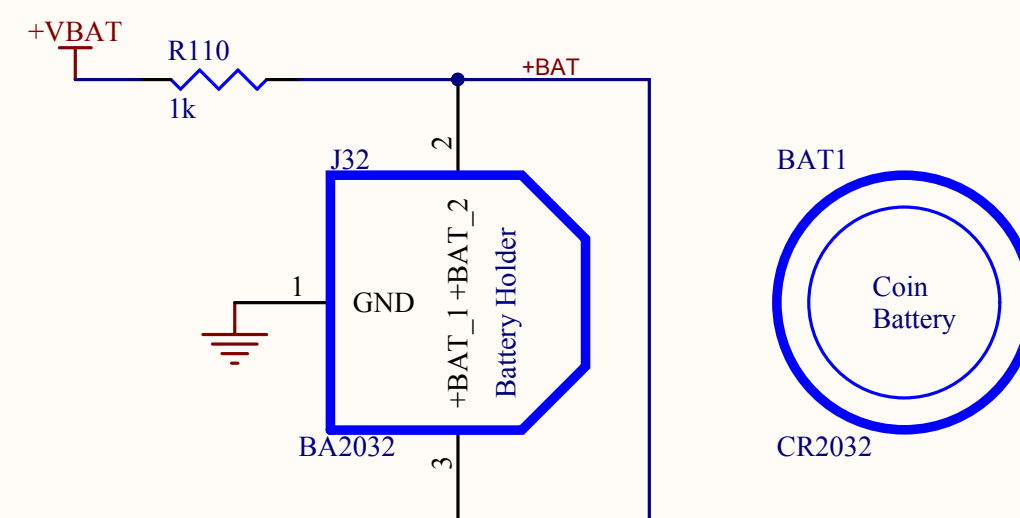
I2C GPIO Expander



EEPROM



RTC Battery

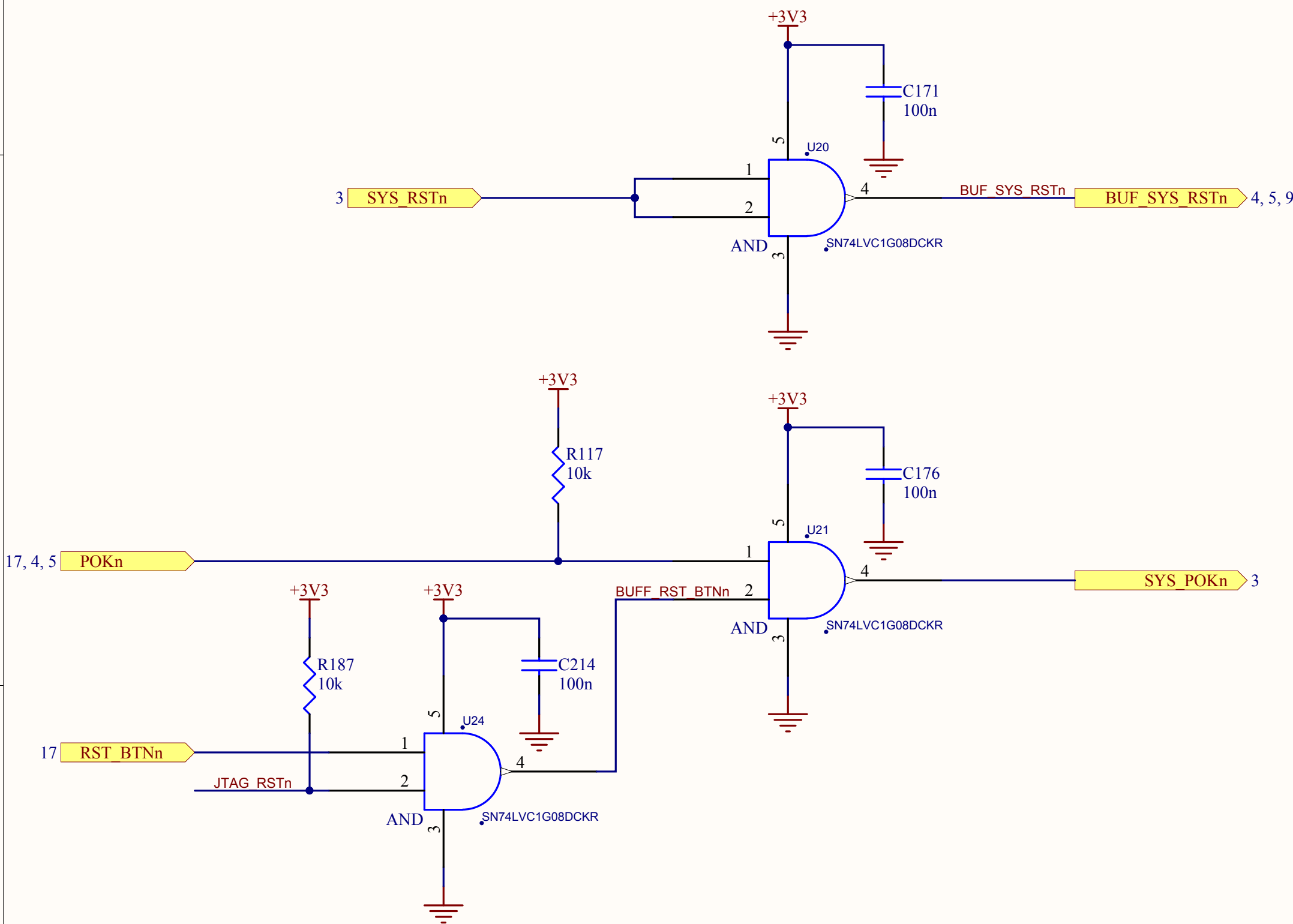


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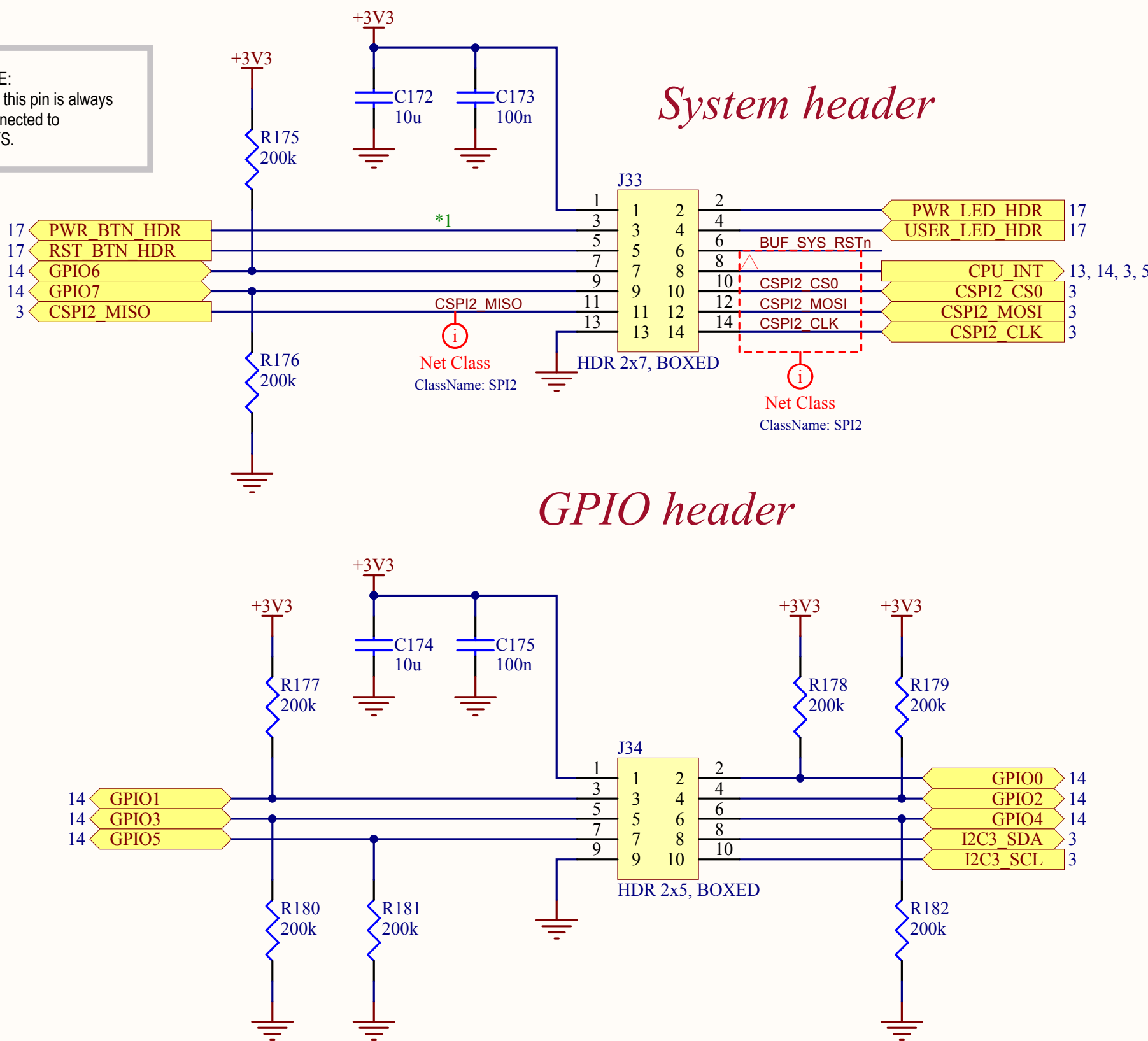
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Page Contents:	[14] - RTC, EEPROM, GPIO, TOUCH SCREEN.SchDocChecked by		
Size:	DWG NO		Revision: V111
Date:	12/3/2013		Sheet 14 of 20

MISC, JTAG, HEADERS

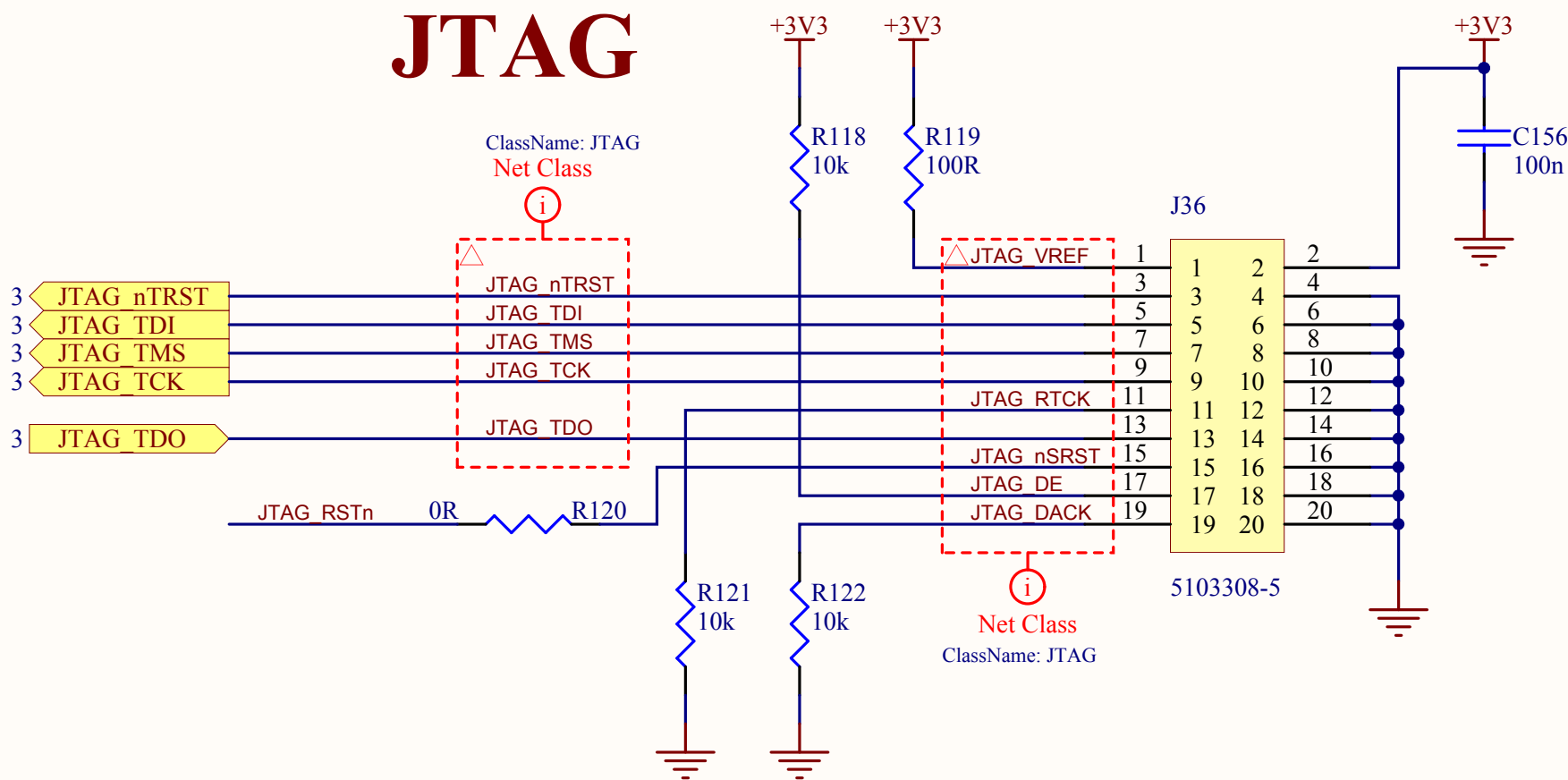
Reset buffers



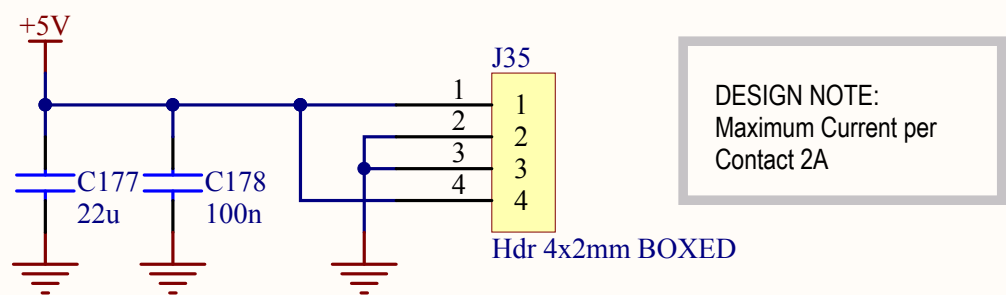
Headers



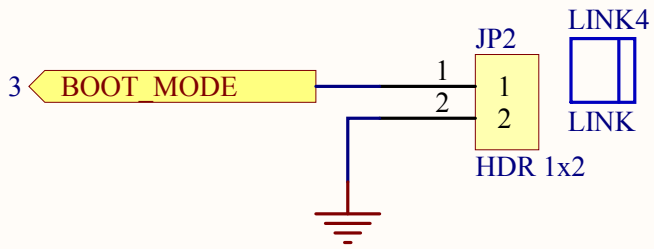
JTAG



+5V Out (For General Use eg. HDD power)



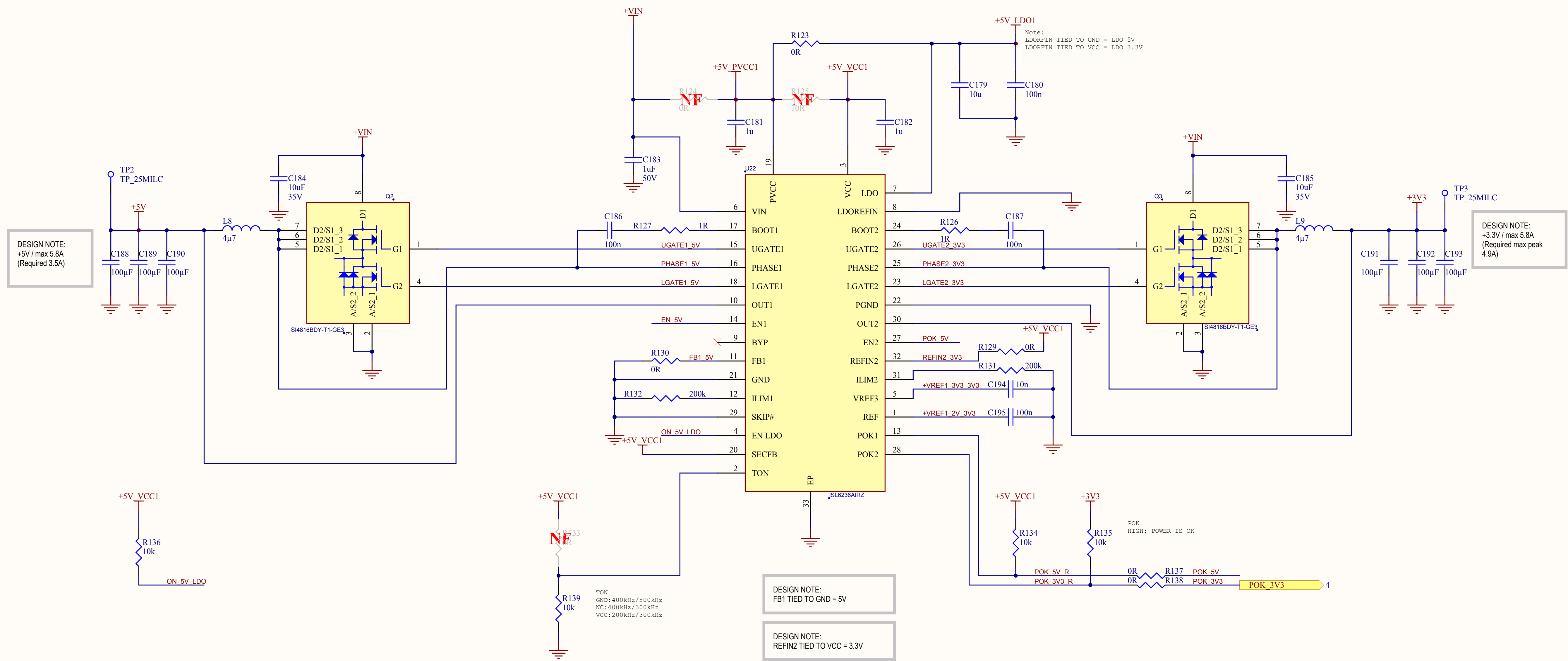
Boot mode selection



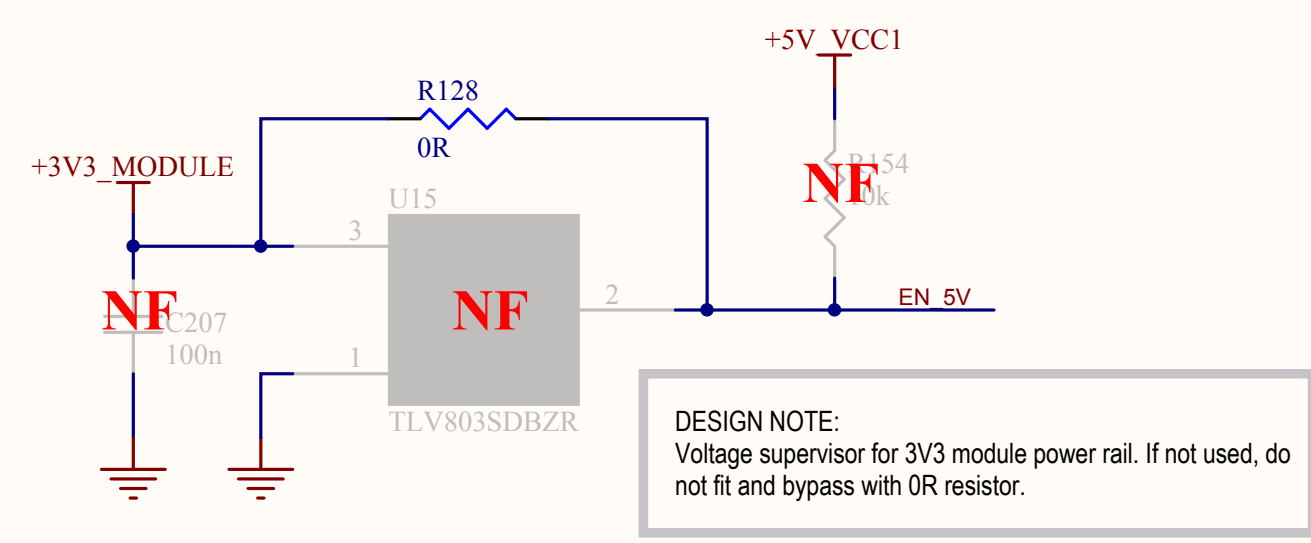
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Page Contents:	[15] - MISC, JTAG, HEADERS.SchDoc		Checked by
Size:	DWG NO		Revision: V111
Date:	12/3/2013		Sheet 15 of 20

POWERS +5V, +3V3



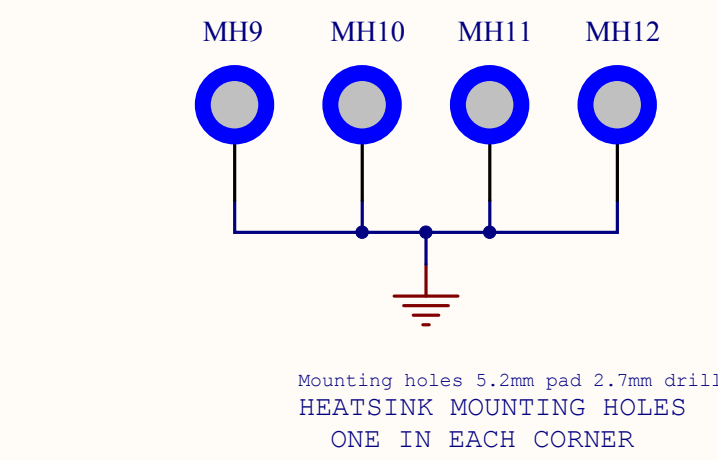
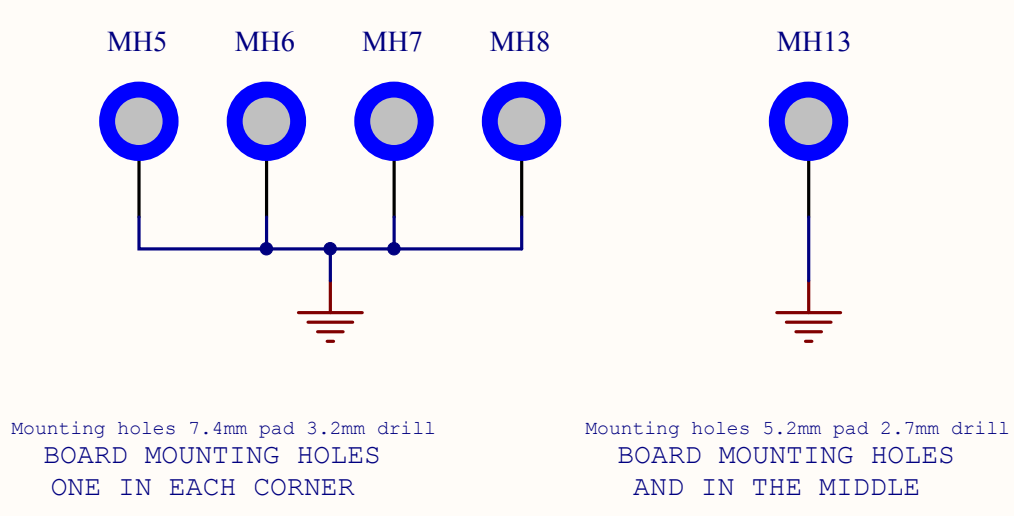
+3V3_MODULE voltage monitor



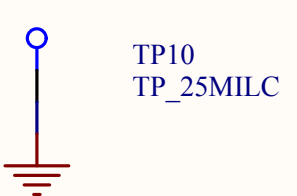
PWR IN, LEDS, BUTTONS, MECH

Mechanical

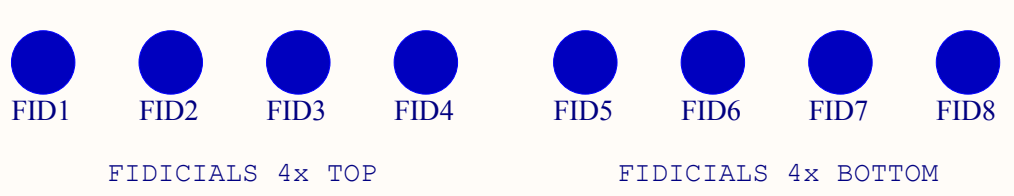
Mounting holes



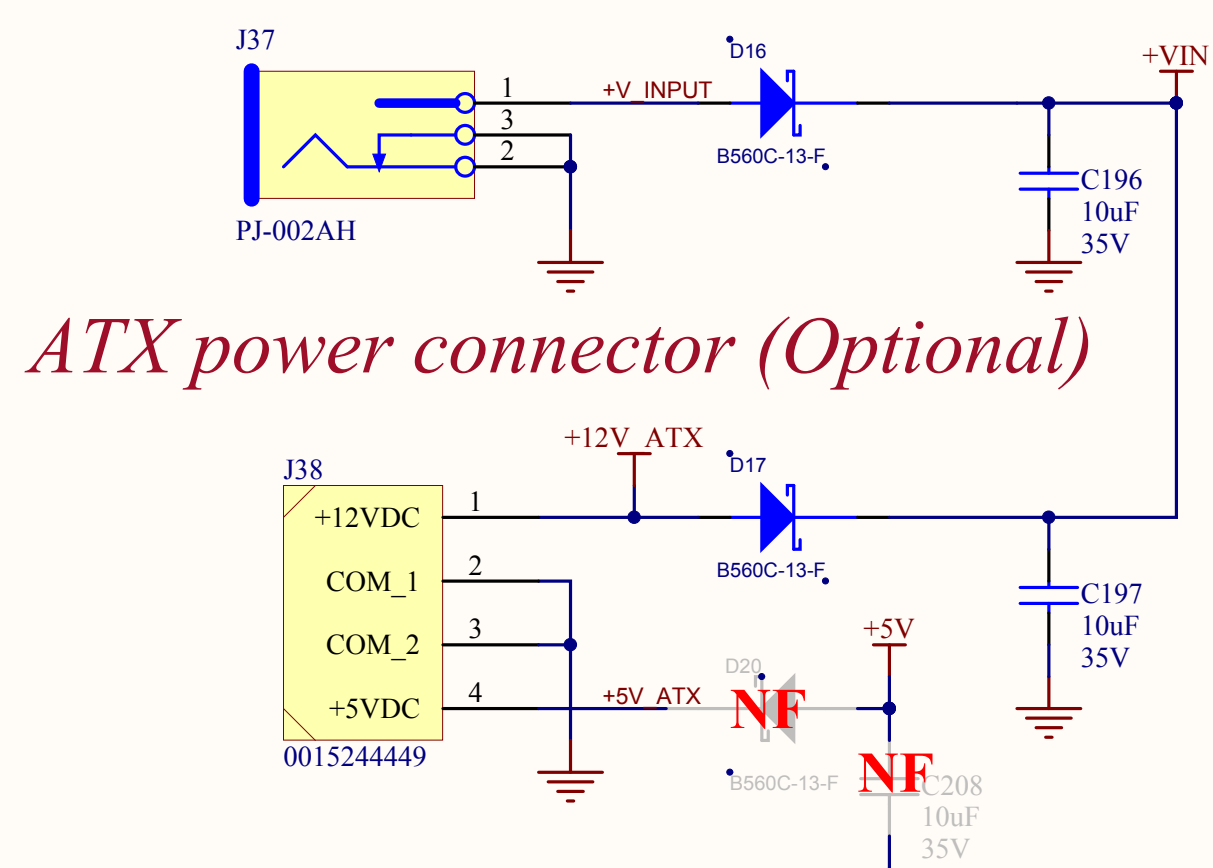
Gnd testpoint



Fiducials



Power Input



ATX power connector (Optional)

DESIGN NOTE:
For automotive application use ATX connector. You can for example place all the required protections on a separate board (e.g. load dump protection) and then connect this baseboard.

DESIGN NOTE:
If ATX connector is used for supplying baseboard with power, fit D17 and C197. If is used as power output then fit D20 and C197. Do not fit both diodes at once!

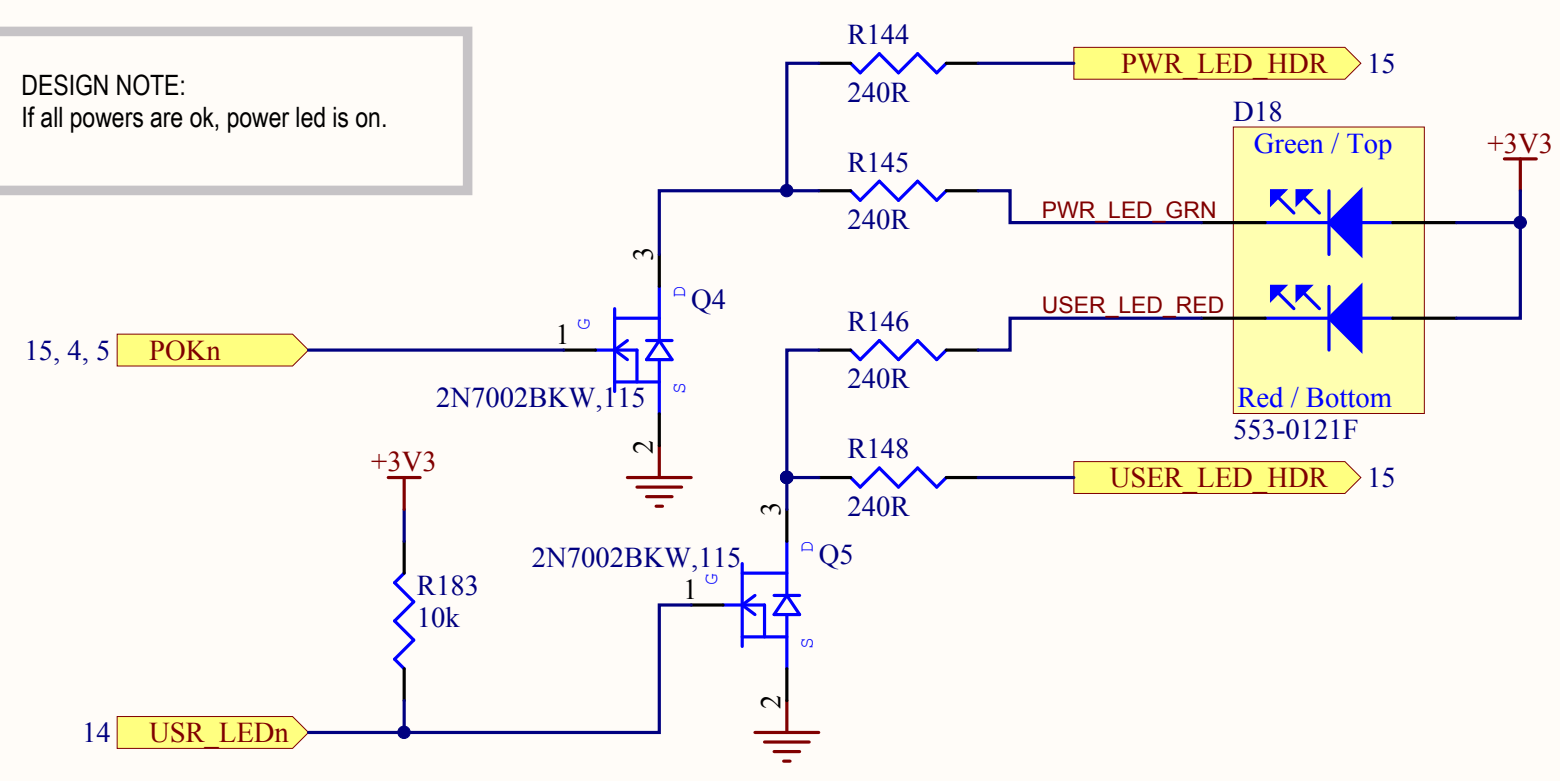
DESIGN NOTE:
If +12V is required by PCIe Card or LVDS Backlight inverter, use ATX connector to power the baseboard.

DESIGN NOTE:
Optional: A 2.5" hard drive can be supplied from this connector (requires only +5V power). Use standard SATA power cable and fit the correct ATX connector on the Baseboard.

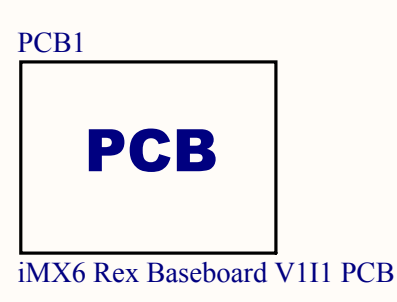
LEDs

Power & Use LEDs

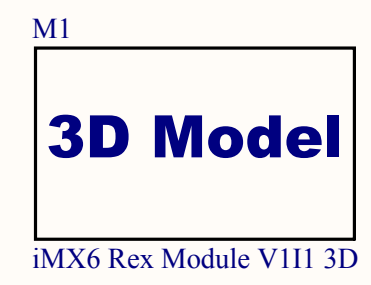
DESIGN NOTE:
If all powers are ok, power led is on.



PCB

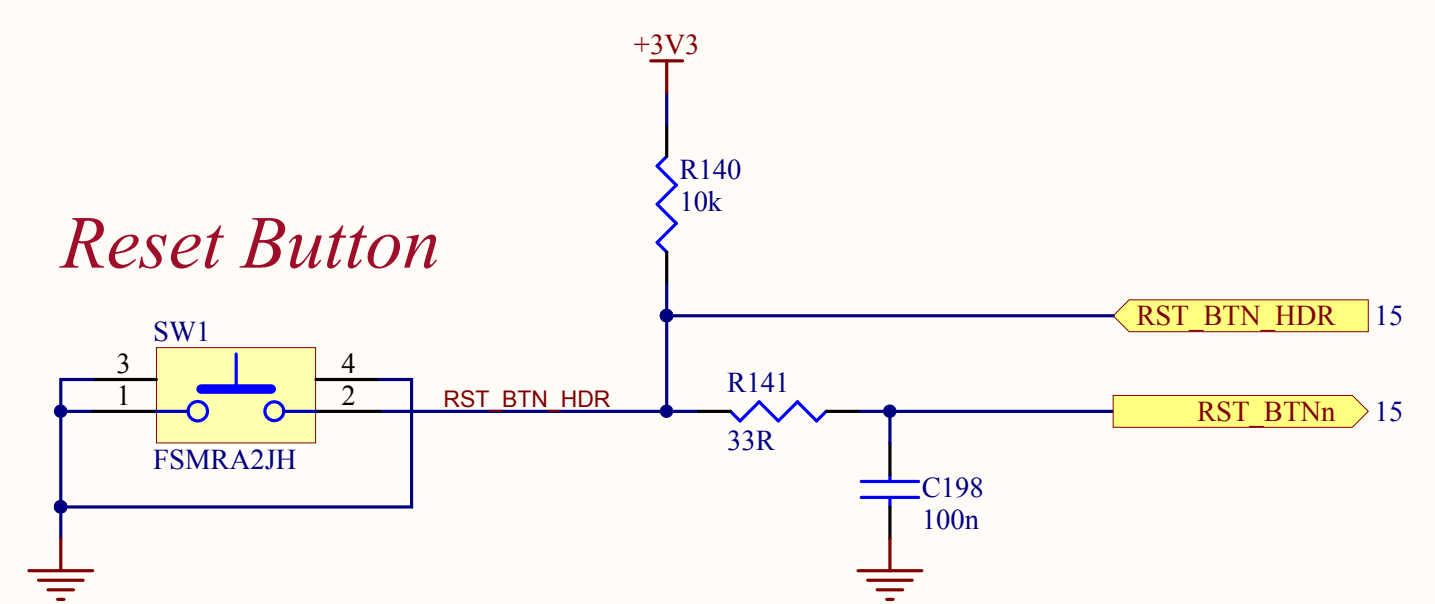


iMX6 Rex Module 3D Model



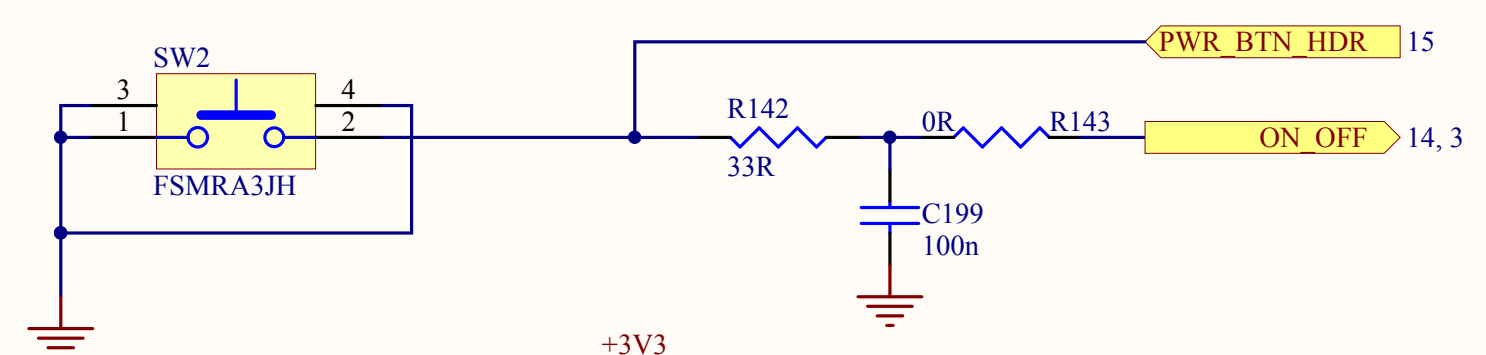
Buttons

Reset Button

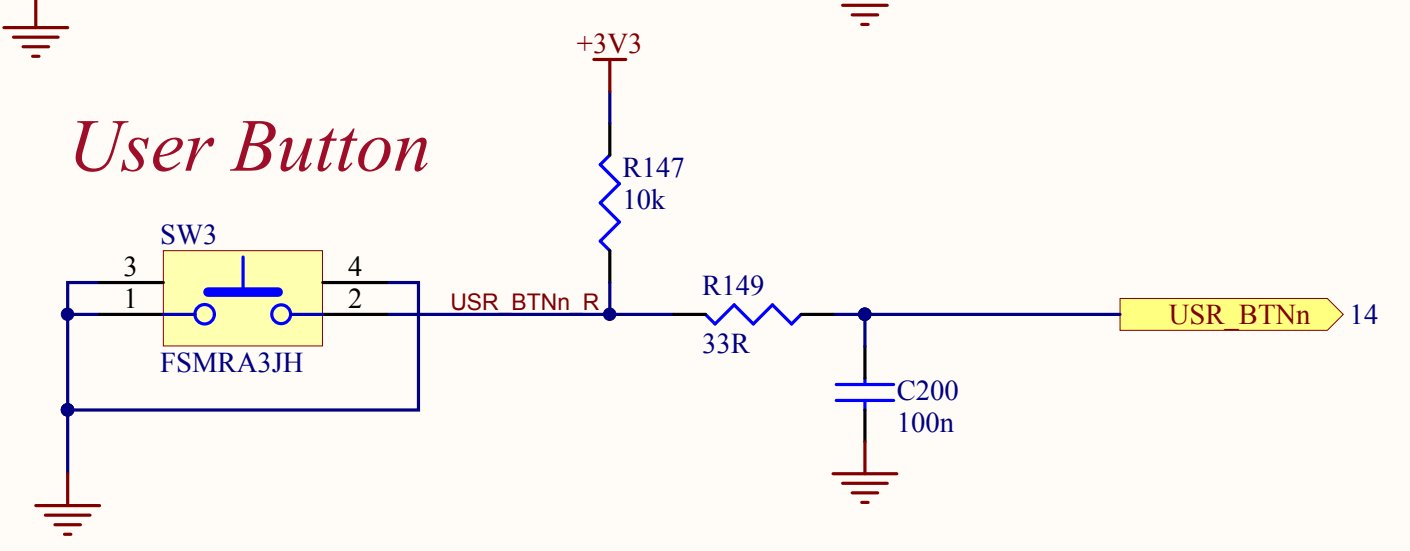


DESIGN NOTE:
Power button has on module pull up resistor (connected to +3V0_ALWAYS).

Power Button



User Button



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Title:	iMX6 Rex Development Baseboard	Variant: Prototype	
Page Contents:	[17] - PWR IN, LEDS, BUTTONS, MECH.SchDoc		Checked by
Size:	DWG NO		Revision: V111
Date:	12/3/2013	Sheet	17 of 20

DOC, POWER SEQUENCING

CONTROLLED BY

NAME

USED BY

POK_1V5

+1V8_AUDIO2

audio

POK_3V3

+1V5

mini PCIe 1, audio

POK_5V

+3V3

peripherals

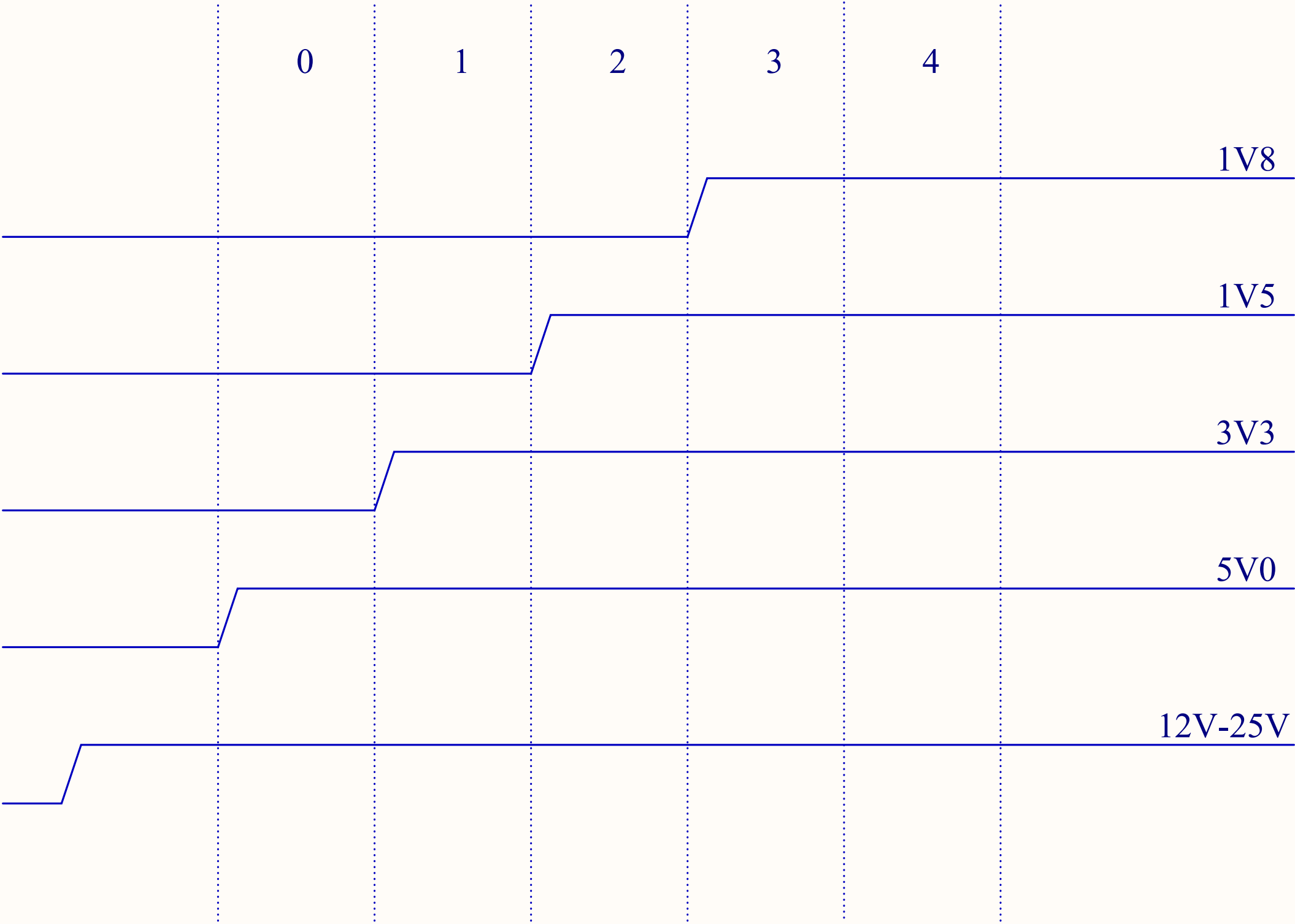
+3V3_MODULE

+5V

USB hub, USB con, backlight

+VIN

switching power supplies, PCIe con



I2C USAGE AND ADDRESS TABLE

NAME	PERIPHERAL	ADDRESS
<i>I2C1</i>	<i>Audio</i>	<i>0x14 / 0x15</i>
<i>I2C2</i>	<i>Audio 2</i>	<i>0x30 / 0x31</i>
	<i>EEPROM</i>	<i>0xAE / 0xAF</i>
	<i>GPIO Expander</i>	<i>0x4E / 0x4F</i>
	<i>HDMI</i>	<i>0x60 , 0xA1</i>
	<i>Mini PCIe / PCIe</i>	
	<i>RTC Clock</i>	<i>0xA2 / 0xA3</i>
	<i>Touchscreen</i>	<i>0x90 / 0x91</i>
<i>I2C3</i>	<i>For general use (On header)</i>	

→ TIME



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Page Contents:	[18] - DOC, POWER SEQUENCING.SchDoc		Checked by
Size:	DWG NO		Revision: V111
Date:	12/3/2013		Sheet 18 of 20

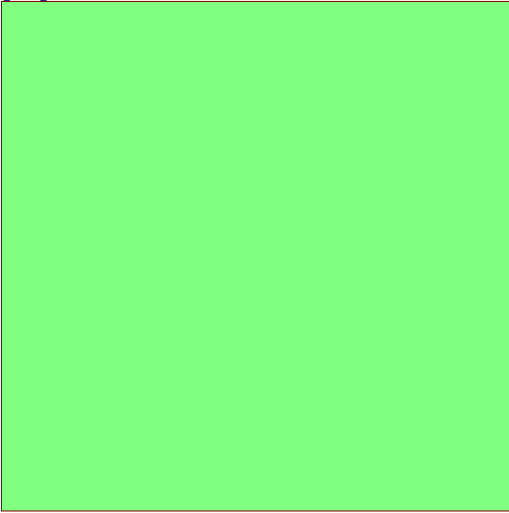
REVISION HISTORY



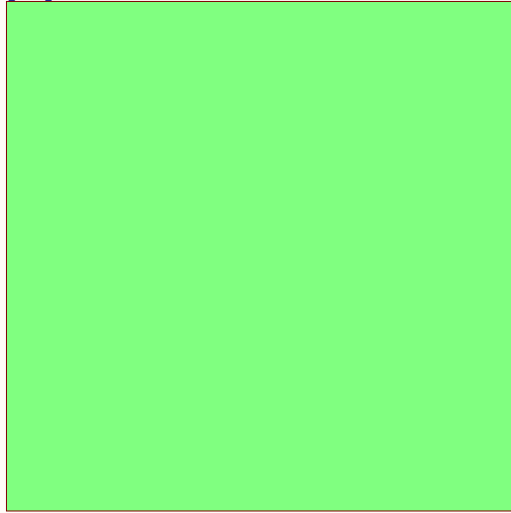
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Title: iMX6 Rex Development Baseboard				Variant: Prototype			
Page Contents: [19] - REVISION HISTORY.SchDoc				Checked by			
Size:		DWG NO			Revision: V111		
Date: 12/3/2013				Sheet 19 of 20			

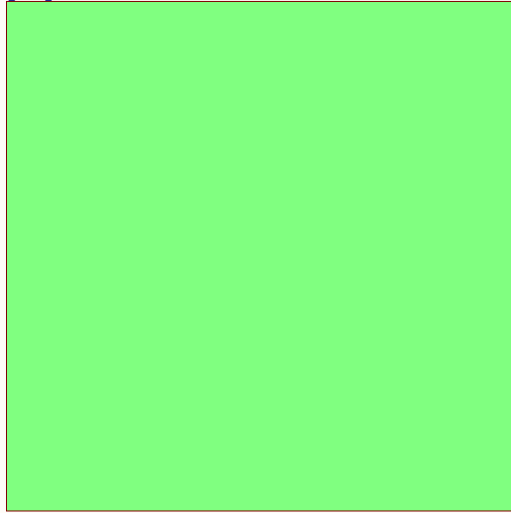
[01] - COVER PAGE.SchDoc
[01] - COVER PAGE.SchDoc



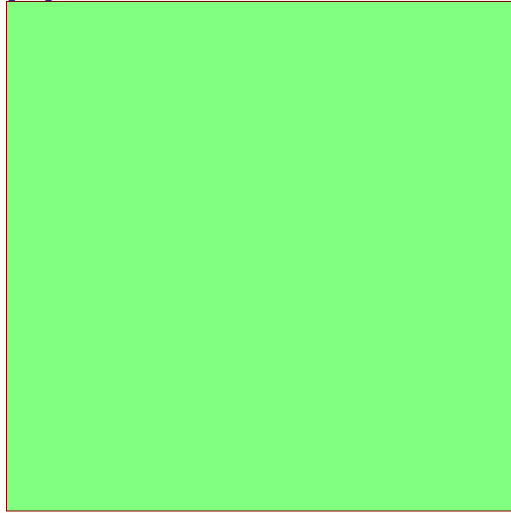
[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc



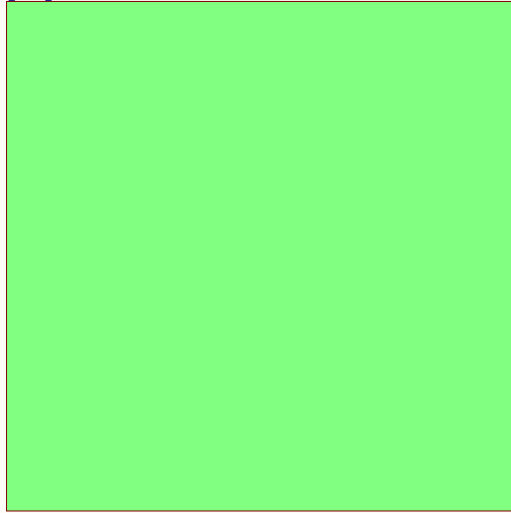
[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc



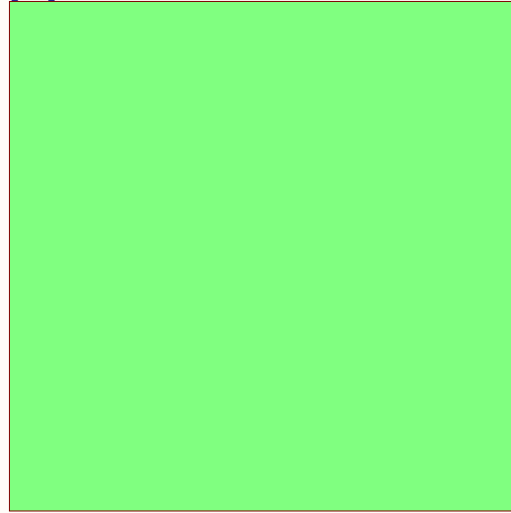
[04] - PCIE MINI 1, PCIE.SchDoc
[04] - PCIE MINI 1, PCIE.SchDoc



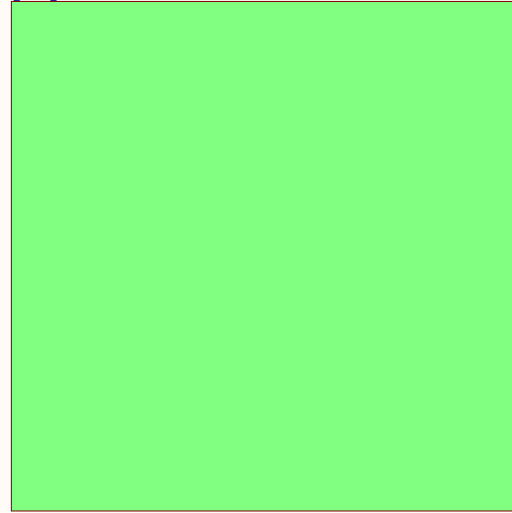
[05] - PCIE MINI 2, AUDIO2.SchDoc
[05] - PCIE MINI 2, AUDIO2.SchDoc



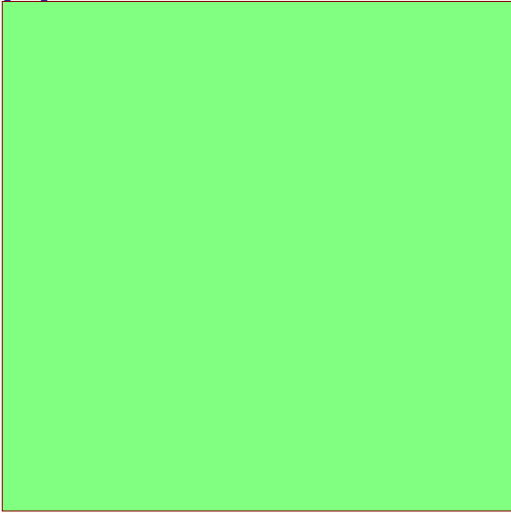
[06] - SATA, CFAST.SchDoc
[06] - SATA, CFAST.SchDoc



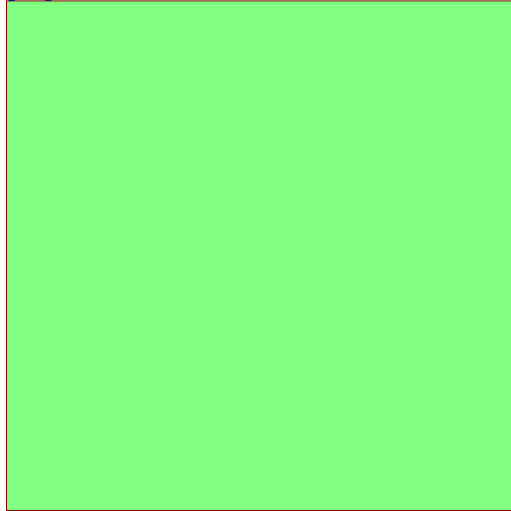
[07] - HDMI.SchDoc
[07] - HDMI.SchDoc



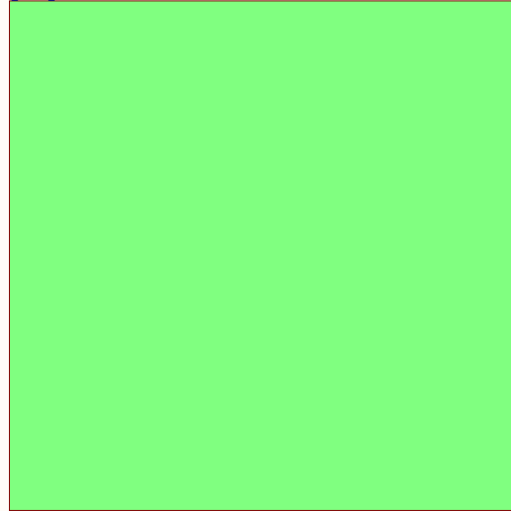
[08] - LVDS.SchDoc
[08] - LVDS.SchDoc



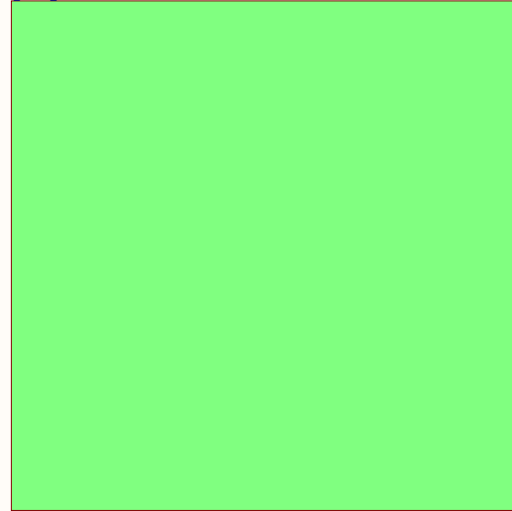
[09] - USB.SchDoc
[09] - USB.SchDoc



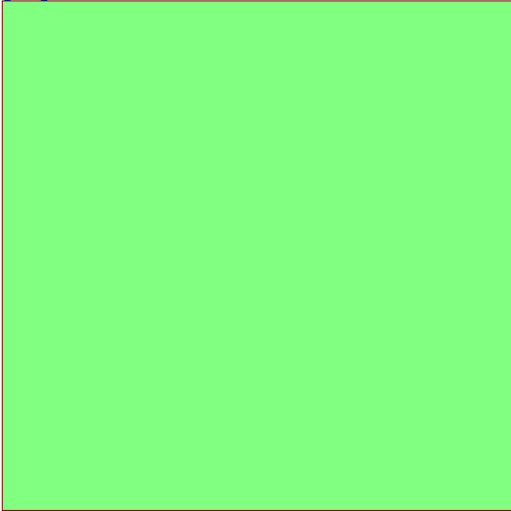
[10] - ETHERNET.SchDoc
[10] - ETHERNET.SchDoc



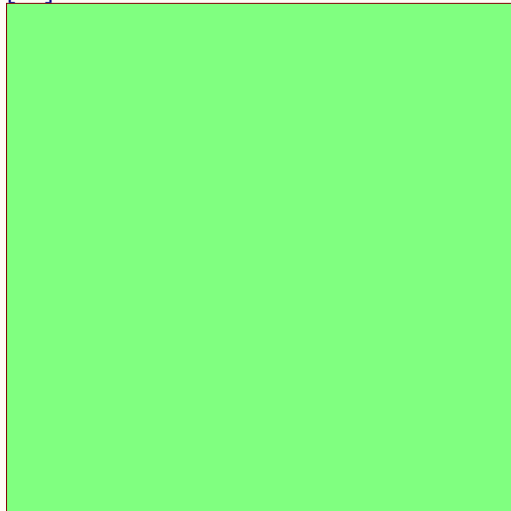
[11] - AUDIO1.SchDoc
[11] - AUDIO1.SchDoc



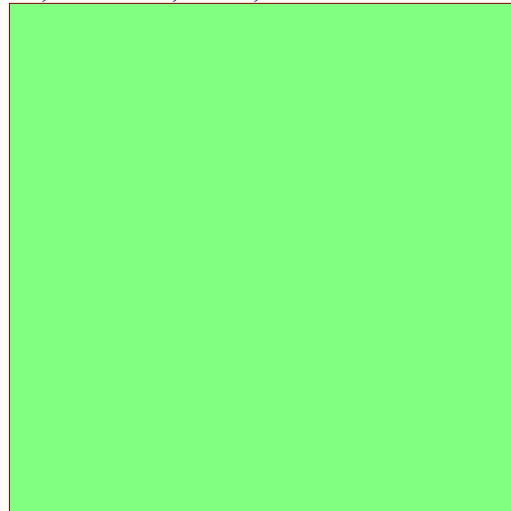
[12] - SD.SchDoc
[12] - SD.SchDoc



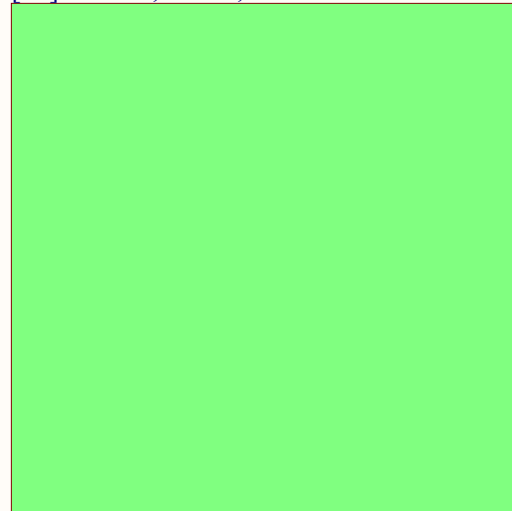
[13] - UARTS.SchDoc
[13] - UARTS.SchDoc



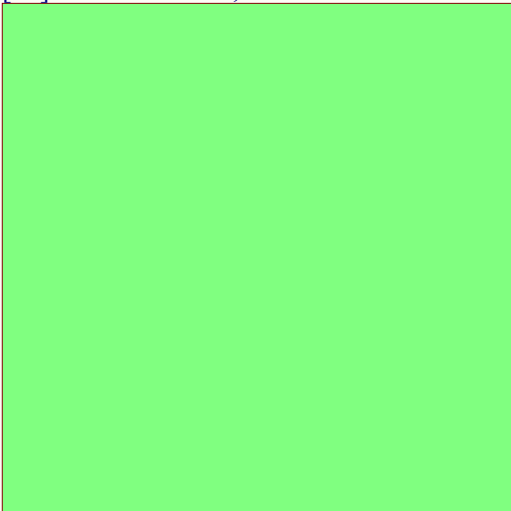
[14] - RTC, EEPROM, GPIO, TOUCH SCREEN.SchDoc
[14] - RTC, EEPROM, GPIO, TOUCH SCREEN.SchDoc



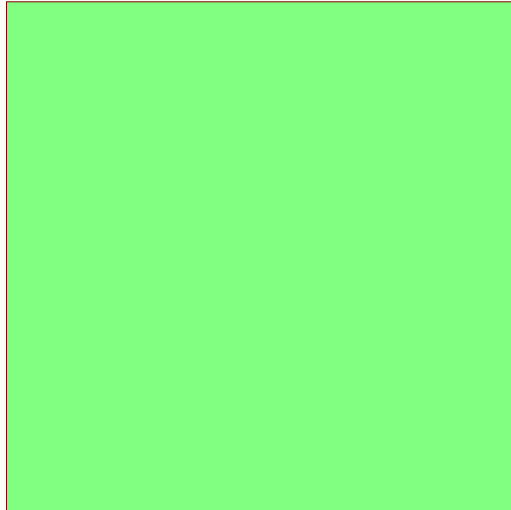
[15] - MISC, JTAG, HEADERS.SchDoc
[15] - MISC, JTAG, HEADERS.SchDoc



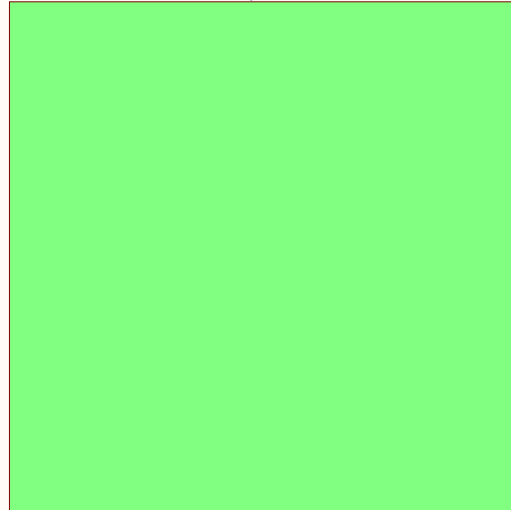
[16] - POWERS 5V, 3V3.SchDoc
[16] - POWERS 5V, 3V3.SchDoc



[17] - PWR IN, LEDS, BUTTONS, MECH.SchDoc
[17] - PWR IN, LEDS, BUTTONS, MECH.SchDoc



[18] - DOC, POWER SEQUENCING.SchDoc
[18] - DOC, POWER SEQUENCING.SchDoc



[19] - REVISION HISTORY.SchDoc
[19] - REVISION HISTORY.SchDoc



TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example



Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Title

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

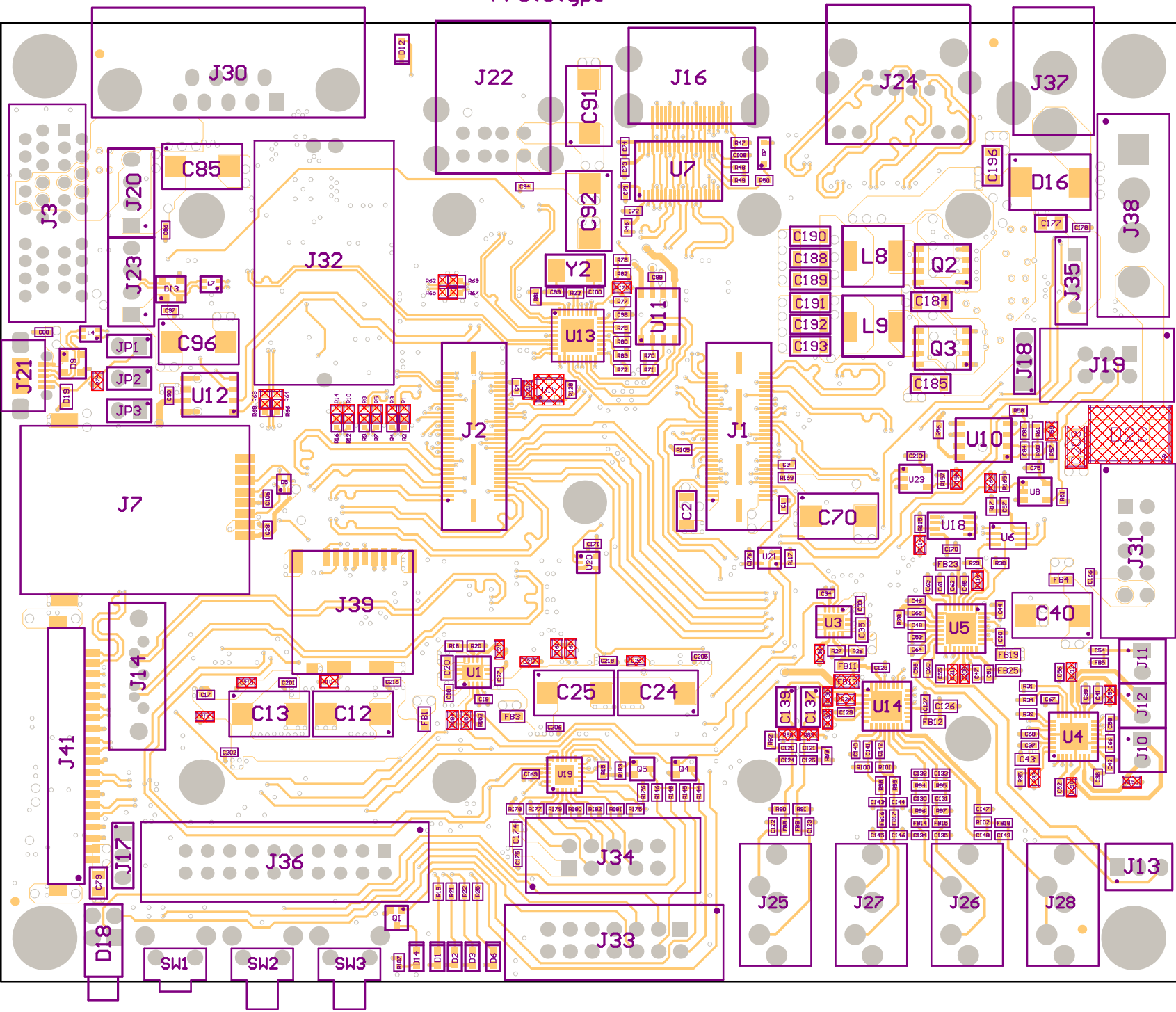


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Title: iMX6 Rex Development Baseboard		Variant: Prototype	
Page Contents: iMX6 Rex Development Baseboard V111 Project.SchDoc Checked by			
Size:	DWG NO	Revision:	V111
Date:	12/3/2013	Sheet	20 of 20

Assembly TOP of iMX6 Rex Development Baseboard V111

Prototype



Assembly BOTTOM of iMX6 Rex Development Baseboard V111

Prototype

