**CONNECTORS**

*Be careful during UART1 signals DSR, DTR, DCD and 100n C240.

**DESIGN NOTE:**
- LVDS0_PWM
- GND

**DESIGN NOTE:**
- UART1 signals DSR, DTR, DCD and 100n C240.

**DESIGN NOTE:**
- TRD0_N
- TRD1_P
- TRD1_N
- HDMI_HPD
- I2C4_SDA
- SD3_CLK
- SD3_WP
- UART1_DTR
- UART1_RTS

**DESIGN NOTE:**
- 10uF
- GND

**DESIGN NOTE:**
- 10uF
- 100n

**DESIGN NOTE:**
- 100n

**DESIGN NOTE:**
- PIC23901

**DESIGN NOTE:**
- I2C1 is used with AUDIO
- 1.0A per contact, 7.8A ground plane

**DESIGN NOTE:**
- Test function of BOOT MODE.

**DESIGN NOTE:**
- USB_OC

**DESIGN NOTE:**
- LVDS0_CLK_N
- LVDS0_TX1_P
- LVDS0_CABC

**DESIGN NOTE:**
- Pic24202
- Pic24201

**DESIGN NOTE:**
- Hardware design courses

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http://www.horad.com/academy/

**Date:** 03.11.2013

**DWG NO:**
When swapping by the lanes on 16-bit memories, remember to move the DQM x.
DESIGN NOTE:
Close to pins +PCIE_VP, +PCIE_VPTX and +PCIE_VPH should be placed additional bigger capacitors. Near these pins are located 4u7 capacitors.
DESIGN NOTE: Glass printed on FR-4 and FEP film should be placed at a distance so that these pins are located out of reach.

+1V1_VDDSOC_CAP
+2V5
R23
R34
220n
C76
22mA
4u7
1k6
+LVDS_2V5
HDMI_RESREF
MCIMX6Q5EYM10AC
NVCC_LVDS2P5
L7
J1
MCIMX6Q5EYM10AC
HDMI_VPH
EIM_DATA18 / ECSPI1_MOSI / IPU1_DI0_PIN07 / IPU2_CSI1_DATA17 / IPU1_DI1_D0_CS / <GPIO3_IO18> / I2C3_SDA
EIM_DATA17 / ECSPI1_MISO / IPU1_DI0_PIN06 / IPU2_CSI1_PIXCLK / DCIC1_OUT / <GPIO3_IO17> / I2C3_SCL
ECSPI1_SS3 / ENET_CRS / HDMI_TX_DDC_SCL / KEY_COL3 / I2C2_SCL / <GPIO4_IO12> / SPDIF_IN
NAND_CE2_B / IPU1_SISG0 / ESAI_TX0 / EIM_CRE / CCM_CLKO2 / <GPIO6_IO15> / IPU2_SISG0

CPU - HDMI, LVDS

i.MX6Q - LVDS

i.MX6Q - HDMI

DESIGN NOTE: Include performance attributes for key

CONFIDENTIAL. Do not distribute.
DESIGN NOTE:
+5V_USB_VBUS should be enabled after +3V3 or after USB0_PWR_EN (USB1_PWR_EN).

DESIGN NOTE:
Resistor R88 fitted, if problem provided by baseboard.

DESIGN NOTE:
+5V_USB_VBUS must be high - DEVICE.
DESIGN NOTE:
All UART signal should be configured in software except UART1_RXD and UART1_TXD.

CPU - UART, AUDIO

UART

AUDIO

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CPU - JTAG, CONTROL

RESET

JTAG

CONTROL

DESIGN NOTE:
Device Design Guide policy not required
(DO CTP).

DESIGN NOTE:
Power ON/ OFF control needs to be tested first.

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CPU - POWER

DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails should be split to the lowest power mode (preventing internal leakage) when using the i.MX6 Dual and the i.MX6 SoloLite processors. VDDARM_CAP should be split to all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection).

LAYOUT NOTE:
It is recommended that the bulk and decoupling capacitors be placed on the VDD/PLL power rails to reduce noise and improve power integrity. The capacitors should be placed as close as possible to the processor.

PROTOTYPE:
A printed circuit board design for the CPU power distribution is shown in this diagram.

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http://www.hedgelockacademy.com
**MECHANICAL**

**TESTPOINT**

**MOUNTING HOLES**

**FIDUCIALS**

**PCB**

**FIRMWARE**

---

**LICENCE**

**ORIGINAL AUTHOR:** FEDEVEL 2013  
**WEBSITE:** http://www.iMX6Rex.com

This is a human-readable summary of the Legal Code (read full licence at:  
http://creativecommons.org/licenses/by-nc-nd/3.0/deed.en_GB).

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<th>Description</th>
</tr>
</thead>
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</tbody>
</table>

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<table>
<thead>
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<tbody>
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</tbody>
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## CPU - POWER SEQUENCING

### OTHER POWERS

<table>
<thead>
<tr>
<th>Name</th>
<th>Level</th>
<th>From</th>
<th>Used By</th>
</tr>
</thead>
<tbody>
<tr>
<td>+USB_VBUS</td>
<td>5V</td>
<td>connector</td>
<td>cpu</td>
</tr>
<tr>
<td>+DDR_VREF</td>
<td>0V75</td>
<td>+1V5_DDR</td>
<td>ref. for DDR memories, gen. with volt. divider</td>
</tr>
<tr>
<td>+1V2_VDD_ARM_CAP</td>
<td>1V2</td>
<td>iMX</td>
<td>cpu, core caps</td>
</tr>
<tr>
<td>+1V1_VDD_SOC_CAP</td>
<td>1V1</td>
<td>iMX</td>
<td>core caps, cpu-sata, cpu-pcie, cpu-hdmi</td>
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</tbody>
</table>

### POWER UP SEQUENCE

<table>
<thead>
<tr>
<th>NAME</th>
<th>LEVEL</th>
<th>USED BY</th>
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</thead>
<tbody>
<tr>
<td>$POK_{3V3}$</td>
<td>+1V2_ETH</td>
<td>1V2, ethernet phy</td>
</tr>
<tr>
<td>$POK_{2V5}$</td>
<td>+3V3</td>
<td>3V3, cpu, pull up</td>
</tr>
<tr>
<td>$POK_{1V5}$</td>
<td>+2V5</td>
<td>2V5, cpu, ethernet phy</td>
</tr>
<tr>
<td>$POK_{1V375}$</td>
<td>+1V5_DDR</td>
<td>1V5, cpu, memory</td>
</tr>
<tr>
<td>$EN_{1V375}$</td>
<td>+1V375</td>
<td>1V375, cpu, core voltages</td>
</tr>
<tr>
<td>+VIN</td>
<td>+3V0_ALWAYS</td>
<td>3V0, cpu, supervisor, pull up</td>
</tr>
<tr>
<td></td>
<td>+VIN</td>
<td>4.75V-25V, switching power supplies</td>
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</table>

### TIME

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>2</th>
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DOC: REVISION HISTORY

01-AUG-2013  Some HDMI and Ethernet signals swapped on J1

19-AUG-2013  Signals for SPI FLASH has been moved to CSPI3

                       Added additional capacitors to +2V5 and +1V1_VDDSOC_CAP

21-AUG-2013  Added resistor from CPU_XTALO to GND

                       I2C3_SDA and I2C3_SCL has been moved to another CPU pins

22-AUG-2013  Always powered voltage change level to 3V0 - supply voltage +3V0_ALWAYS

                       Added bead to connect together +1V2_ETH and +1V375 (Only for testing purpose).

23-AUG-2013  Added resistor to connect SLEEP pin of TPS62175DQCT to +3V0_ALWAYS.

27-AUG-2013  On connector J1 added BOOT_MODE signal to select boot source.
**TEMPLATE NOTES**

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and Version Revision

Mark Not Fitted Components as NF

Net Class Example

Differential signal example

**TITLE Examples (You can change the color to reflect your company color)**

**PAGE TITLE**

*Peripheral / Group of component title*

**Smaller Title**

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.
PRELIMINARY - Close to final schematic.
CHECKED - There should not be any mistakes. Tell the engineer if you find one.
RELEASED - A board with this schematic has been sent to production.

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Assembly BOTTOM of iMX6 Rex Module V1II1
Prototype